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CAD/CAM Feasibility Study

LYNN M. KEUTHAN

Ships Electronic Warfare Systems Branch
Tactical Electronic Warfare Division

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Lynn M. Keuthan

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This report addresses the effectiveness and capabilities of computer-aided design and digitial and analog simulation in an R&D microprocessor environment. The range of tools available, present capabilities of CAD/CAM systems, and complex modeling features are presented and explained. Advanced computer-aided engineering and simulation tools may assist in testing new theories and developing complex hardware and software systems in a more expedient manner.

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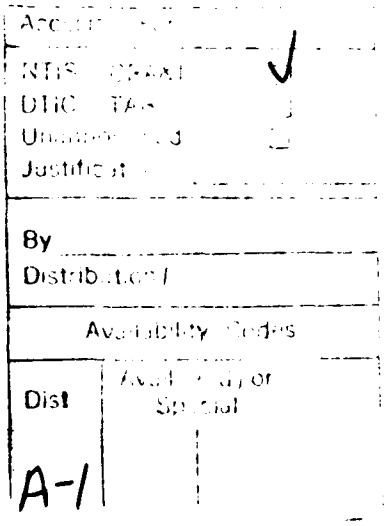

CAD/CAM FEASIBILITY STUDY

FOREWORD

As research progresses and relies on advanced technological tools and as researchers design systems to test theories and to compare techniques, it becomes necessary to expedite the design cycle and to minimize divergences from the central issues of the research programs. For research areas that rely on highly computative processes, digital signal processing (DSP) calculations, and analog waveforms, digital and analog simulation techniques can provide the needed vehicle for analysis.

Digital and analog simulation techniques can be applied to devices ranging from simple logic gates and operational amplifiers to advanced versions of microprocessors and complicated feedback systems. Digital simulation becomes especially valuable when considering complex logic and timing across a board or system level.

In such complex systems, timing problems may occur only when devices operate at the leading edge of the manufacturers' specifications. Likewise, when possible timing hazards are considered, a simulator must distinguish between possible timing problems and problems that would never occur because of gate propagation, common signal origination, or other properties of digital hardware.

The value of digital simulation also becomes obvious when considering the hazards arising from a combination of signals with unknown states, pulses wider than the delay time of a gate, or a combination of both. When a digital simulation system can describe these hazards, pinpoint the origination, and determine whether these hazards persist over a period of time, then the system becomes a reliable and powerful tool for supporting advanced research.

In addition, systems with digital and analog or radio-frequency microwave parts can be difficult to characterize without the use of advanced simulation tools. These complex systems are used, for example, to analyze and develop tracking radar systems. Advanced simulation provides a means for comparing different electronic countermeasure (ECM) techniques.

After comparing a spectrum of designs in simulation, a computer-aided design/computer-aided manufacturing (CAD/CAM) system can readily take the design to printed-circuit-board (PCB) layout. With the proper CAD/CAM equipment, the engineer or researcher can take a design to PCB layout in a relatively small percentage of time and effort.

Simulation results can provide more design reliability than wire-wrap prototypes or even more than the use of a prototype PCB. Further, simulation makes possible the use of new theories and techniques in a testing mode sooner for real world applications and thus provide reliable systems in an expedient manner.

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A designer can spend an appreciable amount of time just in comparing the burgeoning number of CAD/CAM systems available today. Considerable additional time is also required to point out the main features and drawbacks in each system investigated. These procedures have already been carried out in this study. This report includes significant features and explanations of the capabilities of the various available packages used in computer-aided design (CAD).

GENERAL

Computer-aided design and computer-aided manufacturing are subsets of computer-aided engineering (CAE). This report outlines the results of an extensive study on CAD/CAM/CAE systems. Having accepted these definitions, liberty is taken in this report to interchange CAD/CAM and CAE. The report contains a listing of certain companies identified as possible CAD/CAM vendors. Also included is a listing of requirements desired in a computer-aided engineering system.

This report identifies companies that are possible CAD/CAM vendors. A listing of requirements desired in a CAE system is also included. Companies that responded to the feasibility study inquiries are identified. Comparisons are made across all desired criteria for the respondents, and three CAD/CAM solutions are identified with recommendations. These three are compared. Finally, the results of an evaluation of one particular CAD/CAM solution are outlined considering the needs of the Naval Research Laboratory (NRL).

CRITERIA

Having considered all phases of CAD, a list of requirements was developed for CAD/CAM systems. Table 1 lists these phases.

Table 1 — CAD Phases Considered in Developing Requirements

Schematic Entry	User Interface*
Logic Simulation	System Integration
Printed-Circuit-Board (PCB) Design	Maintenance*
Training	Vendor Support*
System Upgrade*	Design Documentation

*Critical areas of concern

To the critical areas of concern listed in the table we must add price per performance. Because of the volatility of the CAD/CAM market and the ongoing state of the art, the ability to upgrade and vendor support are of primary concern and, as such, were weighted heavily in preparing the final analysis and recommendations.

The impressive number of companies entering and exiting the CAD/CAM market illustrates the tremendous degree of competition in these fields and underlines the amount of resources required for designing CAE systems. Overall, however, this market does not seem to favor large companies over small ones. Small companies generally offer systems lower in cost than those offered by long established companies. At this point, the marketplace is consolidating. Company acquisitions in an effort to extend CAD/CAM capabilities or "buy out the competition" actions are numerous. The major CAD/CAM companies for higher end systems are becoming more evident. Companies that provide PC-based packages are numerous, and no one particular company dominates the market. Considering all factors,

the choice of a CAE system for which support can reasonably be assured continues to be difficult and critical.

Companies Polled

The companies polled were principally selected from advertisers in computer magazines over the past five years. Articles listing manufacturers of CAD/CAM products were obtained primarily from Byte Magazine, Computer Design, EDN News, and Electronic Design.

Fifty-seven companies were polled to ascertain whether or not these organizations could meet the desired requirements for CAE development. These companies (Appendix A) were sent a letter (Appendix B) that stated the objective of the feasibility study and listed the criteria (Appendix C) for the study. The letter indicates that the survey is for information only, and not a Request for Proposal (RFP).

Twenty-eight companies answered with some sort of response, only slightly less than half the number of companies polled. A few of the larger companies, notably Computer Vision, G.E. Calma, Hewlett-Packard, and Tektronix, responded individually to each requirement. However, the majority of companies merely provided available literature; individual requirements were not addressed. Only three companies offered products more suited for analog design or analysis: Analog Design Tools, AUTODESK, and Versacad.

Design Computation responded to listed requirements and indicated where their products differed from these. This company also demonstrated flexibility in an attempt to meet additional requirements beyond their current capabilities.

Great Softwestern responded enthusiastically that "we meet this requirement" but failed to provide any supporting literature to verify the statement. What was submitted by this company appeared to categorize the company as functioning more in the role of consultant rather than a system manufacturer. No pricing data were supplied.

Demonstrations and Comparisons

Twelve demonstrations of systems were viewed after the inputs from the 28 companies had been studied and analyzed. Tektronix was found to meet 99.5% of all the stated requirments, and a demonstration was arranged for NRL's Ships EW Branch and other members of the Tactical Electronic Warfare Division. (A copy of the memorandum that listed the specifics of items covered by the demonstration appears in Appendix D.) The percentages of the requirements fulfilled for the various companies were compiled and tabulated (Appendix E) and compared graphically (Appendix F.)

Pricing was compared for the 24 companies that provide digital CAD/CAM systems and cross-compared with the percentage of the requirements met. Pricing is based on basic quotations plus any additional costs for hardware and physical modeling if available and not included in the basic quotation (Appendix G.)

Comparison of Companies

Five companies were found to meet at least 90% of the identified requirements. In order of highest percentage first, these companies are Tektronix, Racal-Redac, Silvar-Lisco, Hewlett-Packard, and Teradyne.

As an example of the market volatility, mentioned earlier, the CAE Systems Division of Tektronix, whose submittal lacked only the desired resolution, was recently acquired by Mentor Graphics. Previous buyers from Tektronix are being phased over to the new owner in a two-year period as all systems are integrated.

Since the takeover, Tektronix has continued to work with the Ships EW Branch to make their original system available at the original price of about $50,000. If the Tektronix system is purchased, Ships EW will be phased over later to Mentor Graphics at no additional cost. The specifics of the transition to Mentor Graphics remain unclear at this time. The new owner plans to adopt the Tektronix ASIC and microwave-design systems because the Mentor Graphics company has no comparable capabilities. Discussions are underway concerning the incorporation of some Tektronix database functionality into the front-end schematic design or, possibly, keeping the Tektronix Database Designer's Schematic Capture (DDSC) as a separate product. Many customers have bought the latter solely for its database functionality.

All of these details imply uncertainties in integration in both Tektronix and Mentor Graphic products. Even those who currently own the Tektronix CAE system may have to contend with inevitably higher maintenance costs and something less than the original Tektronix service.

Racal-Redac, meeting 95% of listed requirements, offers a system for $189,500. This firm has been a major player in CAD/CAM systems for some time and has a steady and well-supported base of customers. A turnkey interface has been maintained to HHB's CADAT (the package known as Visula-CADAT). HHB has added analog simulation capabilities, beginning with the Visula-CADAT version.

Racal-Redac acquired HHB Cadat in 1988. The current company name is Racal-HHB. (The directory in Appendix A lists the headquarters of Racal-HHB as Racal-Redac and the headquarters for the CADAT simulator as HHB-Cadat.) This was a friendly merger caused by the close existing ties between the companies. Both companies realized a tremendous benefit because of an already existing software interface between Racal-Redac's schematic package and HHB's CADAT simulator. This simulator runs on SUN, Apollo, DEC, and PC workstations. Interfaces to HHB CADAT are still available for a number of other packages including those provided by Cadnetix and Computer Vision.

The Racal-Redac system is extremely user-friendly and well integrated. Many industry standards have been adopted (e.g., NFS and SQL) and it is planned to adopt the X-windows operating system interface standard. This system runs on the SUN, Apollo, and VAX workstation platforms. It is extremely versatile and offers a functional solution at a competitive price.

Silvar-Lisco supplies 92% of the requirements with their CAD/CAM system. Extensive software packages are available for CAE applications. This company is traditionally known for ASIC design rather than PCB design and may have geared its products for ASIC design and development.

Silvar-Lisco also compares well in the needed technical requirements for CAD and development. Some concern exists, however, about the availability of reliable support and service. The company seems to expect the customers to travel to their facility in Nashua, New Hampshire, for product demonstrations. Initially, the company was reluctant to provide any pricing data in the absence of a formal RFP but finally provided the information that their software is licensed for a base fee of $79,000 to which $11,850 is added to cover maintenance. These figures do not include hardware costs, and the charges are assessed on an annual basis.

Hewlett-Packard, meeting 91% of the stated requirements, offers a well-integrated system for schematic capture, logic simulation, and PCB design. Gen-Rad's HILO-III is integrated to their schematic and PCB products to assure logic simulation capability.

The logic simulator HILO-III addresses each requirement for logic simulation in conjunction with a physical modeler, HI-CHIP. The package is available from Hewlett-Packard for $69,200. The additional HILO-III cost of the HI-CHIP physical modeler depends on the particular device support required.

Logic Automation intends to support HILO-III soon with their physical modelers. GenRad had discontinued adding devices and upgrades to their HILO-III during the last two years, but lately efforts have been resumed in research and development aimed at updating GenRad's model libraries for this product.

Hewlett-Packard also addresses many of the desired features of a CAD/CAM system. They provide excellent front-end database management capabilities not available elsewhere. The designer can add information fields to a schematic design. However, Hewlett-Packard is lacking in the areas of open architecture, versatility, and flexible configuration.

The Hewlett-Packard package runs solely on the HP9000, Model 350 workstation. This closed architecture does not allow networking to other workstations or the transferring of files. Not only is the choice of platforms limited but hardware interfaces are also limited to their own plotter, printer, and software development station. This can add considerable additional expenses in hardware.

At this time, high-quality Houston Instruments plotters and a number of printers have been procured and are available to the Ships EW Branch. Additional procurements have been placed for needed software development tools that were selected as the best technical solution and the most cost-effective. Hewlett-Packard provides no support in addressing interfacing needs to other systems. A designer's board-application code can not be easily downloaded to a development station other than one made by Hewlett-Packard. This vendor's station costs about $60,000.

Without HI-CHIP, Hewlett-Packard's CAD/CAM system can be purchased for $138,411. Although the company claims to be moving more positively in the direction of open architecture, the requirement for interface with their proprietary equipment still exists.

Teradyne meets 90% of specified requirements. They provide extensive and elaborate tools for CAE. Such tools include schematic capture, logic simulation, physical modeling, PCB design, thermal analysis, and extensive production board testing devices. Teradyne has recently acquired Case Technology and AIDA, thereby broadening its base in many phases of CAE.

Teradyne has well-developed business relationships with board-testing and computer-manufacturing companies. These relationships permit the company to address many questions relating to the interfacing of their equipment (e.g., with Tektronix DAS 9200). Teradyne has also a history of joint demonstrations with Digital Equipment Corporation.

Teradyne offers some of the most sophisticated logic and fault simulation tools available. Appendix I provides a selection of their logic simulation features.

Teradyne's logic simulator, LASAR, detects many possible logic-design problems that could otherwise not be detected until many production boards had been delivered to the field. The cost of this

system, $180,300, excluding hardware, is justified by the tremendous system features and customer support available.

Companies Meeting Fewer Requirements

Four more companies meet at least 80% of the listed requirements. With their respective percentages these are: Computer Vision, 88%; Mentor Graphics, 87%; G.E. Calma, 82%; and Scientific Calculations, 81%.

Computer Vision, boasting the most sales in CAD/CAM development, supplied the most elaborate data package. Each requirement was specifically addressed, and prices were given; installation requirements were defined, and sufficient additional information was provided to enable the actual purchase of the package.

The company interfaces with HHB's CADAT for logic simulation. To purchase this package through Computer Vision, the applicable price is $25,000 with an additional $129,059 for the HHB CAT hardware modeler. Another additional cost of $99,800 for hardware and software support of PCB design is difficult to justify; the company develops only schematic capture and PCB-design software.

Mentor Graphics has a product that runs on the Apollo* with the addition of certain proprietary hardware; the system has a closed architecture. No high-level language interface is provided for changing schematics or for writing simulation files. Since their software has controls built in to maintain a proprietary system, ASCII files from a designer's program code cannot be easily transferred to a development station for either debugging or for PROM burning (or vice versa for simulation). All these factors limit flexibility in a research-oriented environment.

The Mentor Graphics system is sold as a "designated workstation." This means that software installed on one particular workstation cannot be accessed from another workstation. When designing schematics, a "schematic-capture workstation" must be purchased. Essentially, software is licensed to the one workstation and for any software on that workstation to be executed elsewhere, a unique workstation must be acquired.

Mentor Graphics' complete CAD/CAM package can be purchased for about $250,000. NRL's EW Support Measures Branch is currently using this company's CAD/CAM system. Should Ships EW Branch wish to network to this existing system it would be necessary to purchase another complete pckage at $250,000 and a $6,000 cable to connect the two workstations. The only possible plus in making such an arrangement would be that Ships EW Branch would have access to the other branch's high-quality plotter.

Mentor Graphics has made a number of acquisitions recently. These include the Tektronix CAE Division and Silicon Compiler Systems. Both of these acquisitions were strategic, buying out competitors to the Mentor Graphics product line. No previous interfaces existed to the CAD packages produced by these companies, and products overlap in functionality; the completion of integration will be difficult. Mentor Graphic's attempts to "corner the market" will not necessarily produce a better CAD/CAM package for its customers. Since the CAD/CAM package, which originated with Silicon Compiler Systems, Inc., runs on the SUN workstation, Mentor Graphics hopes also to port its CAD/CAM package to this platform.

*It should be noted that Apollo was recently acquired by Hewlett-Packard.

The advantage of using Mentor Graphics' software for all areas of desired CAD/CAM development (schematic capture, logic simulation, and PCB design) is compromised by limitations in the closed architecture and in the use of proprietary hardware. Competitive products that specialize in a particular phase of computer-aided design surpass Mentor Graphic's performance in these phases.

The G.E. Calma system offers schematic capture and PCB design capability for interface with HHB's CADAT. However, the latter must be purchased from HHB and then integrated with the Calma product. This product runs on both the VAXStation and Apollo workstation; it was available for about $172,000 at the time of this CAD/CAM survey.

General Electric Company sold the G.E. Calma operation in 1988. The CAD portion was sold to Structural Dynamics Research Corporation (SDRC); the remainder was sold to Computer Vision. G.E. at one time held a controlling interest in SDRC. At that time, SDRC supplied CAD software to G.E. The latter then integrated it with their CAD/CAM products. In 1988 SDRC bought back stock held by G.E. SDRC uses the CAD video terminals and the software bought from G.E. for drafting, solids modeling, finite-element analysis, test data, and plastics design application software.

Scientific Calculations was one of the first companies to enter CAD/CAM development. They provide an extremely powerful and user-friendly package for schematic entry and PCB design, SCICARDS.

Recently, Scientific Calculations introduced a new package called MicroCARDS, which was designed for the novice designer. This package continually offers menus to the designer, thus allowing the choice of various options. This format is particularly useful in PCB design work, stepping the designer through a complete board layout.

Scientific Calculations fails, however, to provide some newer features of CAD/CAM development. These include a high-level language interface, manipulation of board application code in standard ASCII files, and interfaces to testing equipment. Another drawback is that the package cannot be purchased outright. It is available only by licensing. The licensing fee is $100,000 up front and $1,000 a month afterward. These charges do not include interfacing to logic simulation or the cost of hardware. If the system is not heavily utilized and if Scientific Calculations does not add the newer CAD/CAM features, the package represents a rather expensive investment.

Cadnetix, meeting 71% of listed requirements, claims that their product is aimed toward ASIC design rather than PCB design.

PC-Based Systems

When all available PC-based products are compared, few truly stand out as versatile and widely used. Some PC-based companies have tried to "pseudosimulate" mainframe world capabilities. These companies tend to offer substandard products across the areas of schematic capture, logic simulation, and PCB design. Where schematic design alone is considered, three PC-based companies are noteworthy: Case Technology, OrCad Systems, and Personal CAD Systems.

Case Technology meets 99% of schematic capture requirements. It was recently acquired by Teradyne, a company that, as we have seen, produces the LASAR logic simulator. Therefore, Case Technology's package can no longer be purchased with HHB's CADAT simulator. The only common platform presently available between Case Technology software and LASAR is the VAXStation platform, making the Case PC-based platform unusable with logic simulation. At this writing, Teradyne has no plans to port LASAR to the PC.

OrCad Systems meets 89% of schematic capture requirements; Personal CAD Systems meets 84%. Both packages are well developed and accepted in the marketplace; both are extremely user-friendly.

Comparing the respective packages produced by OrCad Systems and Personal CAD Systems, only OrCad provides standard interfaces. One of the more common of these is their FutureNet netlist. This package provides a turnkey interface to HHB's CADAT. Other interfaces include those to PCB packages of Computer Vision, Scientific Calculations, and CAD Software. It is also noted that OrCad has established and maintained good customer support.

One of the oldest PC-based companies in the market is FutureNet, which was recently acquired by Data I/O. FutureNet, often noted for its schematic entry package, has been interfaced to a number of other CAD/CAM products. Fortunately, this situation has provided a standard interface for companies producing PC-based software packages, just as IBM, with its early entry into the PC-computer market, established standard PC operating system interfaces.

Recently, FutureNet was compelled by Data I/O to redesign its schematic entry design. As a result, FutureNet no longer provides upgrades to its schematic-entry packages, although earlier this was their strong point in selling to long-held customers.

About a year ago, Data I/O/FutureNet produced a back-end PCB product to interface with their schematic entry design. Recently, this was taken off the market. Even in the schematic-entry front-end, the FutureNet package tends to be difficult to work with, and not as sophisticated as other available packages.

Additional Companies

Two companies, Daisy Systems and Valid Logic, which have made a name for themselves, failed to respond to the invitation to participate in the feasibility study. Two contacts in Valid Logic, made earlier, have left that company. The more useful of these two is now with Digital Equipment Corporation (DEC). Recently DEC was used as a beta test site for Valid Logic. The latter company appears to be short staffed.

Although Daisy Systems has long portrayed itself to be a PC-based company, this company has always required additional proprietary hardware to operate on the PC. This hardware places the company on a closed-architecture platform at the price of a standard stand-alone workstation such as the Apollo workstation or DEC's VAXStation. In an effort to enter the standard workstation market, Daisy advertised compatibility with a VAX platform. In this system configuration, all software was based on the PC and the main function of the VAX was to serve as a file sorter. This is a rather expensive application for a VAX.

Another company that failed to respond to the invitation to participate in this study was CAD Software, Inc., a newer company in the CAD/CAM market. The president of this company was formerly with Racal-Redac along with a number of CAD Software employees. At this writing, it is only known that the company does have a PCB package on the market.

At NRL, the Engineering Services Divison (ESD) has purchased six software packages from CAD Software. Designers previously using Racal-Redac for PCB design are now waiting in line to use the PADS PCB package from CAD Software. This package claims to interface with a number of schematic-entry packages, including those offered by FutureNet and OrCad. ESD is currently interfacing PADS PCB with OrCad.

PADS PCB is an extremely powerful PC-based package. When interfaced with a schematic-entry package, it provides automatic wire connections and pin-outs. PADS PCB also includes powerful auto-placement and auto-routing software. Their auto-routing package includes a sophisticated "rip-up" router that continues to rip-up and reroute a board until the operation is successful. This PCB package is priced at $5,475.

Logic Simulation Systems

William D. Billowitch, Executive Vice President of Quadtree Software, as quoted in Appendix H, notes that simulating board design can have many benefits beyond simply developing a breadboard. Simulation, he points out, saves considerable time and money in the testing phase. Simulation techniques not only verify logic design but provide timing analysis and fault simulation, and also significantly increase the level of complexity available for verifying designs. In the present areas of concern at NRL Ships EW Branch, this offers invaluable capabilities for dealing with microprocessor and simulation research.

Many levels of logic simulation are available for ASIC and board-level design. They include structural (gate) level, behavioral modeling, and physical modeling. Gate-level simulation involves modeling simple gate structures such as "AND" and "OR" gates or flip-flops. This level of simulation is the most simplistic and detailed, therefore it results in the slowest speed of execution. At the microprocessor level, gate simulation becomes impractical and unavailable.

Behavioral models are used most commonly in logic simulation. Implementing behavioral models requires an understanding of the functionality of the device being modeled. Sophisticated logic simulators provide comprehensive behavioral-model libraries. Many also allow a designer to build a unique behavioral model, using a high-level language such as C or a company-designed C-like language.

Hardware models use the actual device as the simulation model. By so doing, a designer is assured of an accurate logic model. Timing accuracy, however, must sometimes be limited by economic factors. This can lead to producing inaccurate timing analysis. Because of the need for communication between the hardware modeler and the simulator and scheduling of hardware models, the timing of the hardware-modeled device is slowed down to approximately the same speed as that of the logic simulator software model. Hardware models do provide the most accurate simulation for complex VLSI devices.

Testing complex board designs becomes possible through fault simulation. Test patterns can be developed by creating a simulated circuit, drawing an applied waveform, or specifying applied test patterns. After testing and verifying the design logic of a circuit, a designer, through fault simulation, can test the design further by injecting (imposing) faults at the simulation inputs. A designer, through concurrent fault simulation, can consider and rapidly test for the occurrence of the most likely combinations.

Also necessary in any true logic simulator is the need for simulation of random-access memory (RAM), read-only memory (ROM), and programmable logic devices (PLDs). Simulation is implemented through high-level language files that allow a designer to easily modify the program code or the PAL logic. Typically, this is a time-consuming task if done by breadboarding a design.

Logic simulators also give a designer unlimited capability to monitor timing signals. Generally, CAE tool sets have a bandwidth equal to the timing resolution of the simulator, generally less than 1 ns. In addition, unlike a logic analyzer, triggering is automatic, allowing every signal to be monitored.

Available Logic Simulators

Several PC-based companies claim to have logic-simulation capabilities. These include OrCad Systems, Personal CAD Systems, Spectrum Software, Viewlogic Systems, and Visionics. All of these packages tend to have simplistic timing analysis at best. PCAD, offered by Personal CAD Systems, even requires a designer to input the logic for simple "AND" and "OR" gates to create the applicable logic simulation. Only OrCad and Viewlogic claim the capability for RAM, ROM, and PLD simulation. Not one of these packages has the capability to do behavioral modeling, physical modeling, or fault simulation.

Appendix I notes that timing analysis becomes more of a hindrance than a help if the analysis produces timing errors that would actually never occur in real life. This can occur if the logic simulator does not take into account such items as common ambiguities between signals, correlation, and glitch analysis.

Common ambiguities occur when two signals reconverge from a common point in the circuit. A common delay has been added to both. Only sophisticated simulators can detect this. Only two logic simulation companies have addressed this point in this study: Teradyne with its LASAR simulator, and HHB with its CADAT simulator.

Also, both companies address correlation and glitch analysis. Correlation techniques take into account that certain gate structures tend to "follow" one another through a circuit; therefore, certain min/max timings never occur in the real world. Not only do LASAR and CADAT allow the setting of various min/max combinations, but they actually put together the most typical combinations likely to occur.

As for glitches, many higher-end logic simulators either report all the glitches occurring in a design or allow a designer to specify the smallest-width glitch to report. So specifying does not guarantee that glitches narrower than the width specified will not cause failures in board design. These two approaches can either create an overly pessimistic simulation analysis showing glitches that would not affect actual board performance, or overlook glitches that might well cause design problems. Only Teradyne's LASAR completely addresses these simulation problems and identifies glitches with detailed "hazard" reports which allow a designer to make an appropriate decision on whether a timing violation has, in fact, occurred.

Looking at the cost of the various packages which meet necessary logic-simulation requirements, only the HHB CADAT costs less than $200,000; this version is available for about that amount. Only four of six available simulators meet the requirement cited in this study for support of recent developments in IC and, in particular, support VLSI devices. Among these, only CADAT offers the widest range of platforms, including Apollo, VAX VMS and ULTRIX, SUN, PC, and HP. Table 2 presents a summary of information pertaining to these packages.

Physical Modeling Capabilities

Of the six companies offering logic simulation, only HHB and Teradyne offer physical modeling capabilities directly. The others rely on such physical modeling companies as GenRad, Quadtree Software, and Logic Automation. HI-CHIP, GenRad's physical modeler, sells for $69,200. Tektronix (as previously stated, the CAE Division was recently acquired by Mentor Graphics) and Hewlett-Packard sell HILO-III and HI-CHIP as options for their CAD/CAM packages.

Table 2 — Software Packages Meeting Logic-Simulation Requirements

Company	Package Name	Remarks*
GenRad	HILO-III	3
HHB Systems	CADAT	1, 3
Mentor Graphics	Mentor Graphics	1, 2
Silvar-Lisco	LOGIX-SL	1, 2
Teradyne	LASAR	1, 2

*Remarks
1. Provides simulation of recent IC developments
2. Interfaces solely with own front-end proprietary packages
3. Interfaces with multiple CAD/CAM systems

Quadtree Software provides the most accurate physical models for microprocessors. Quadtree Software models are "certified," which means that the device manufacturer of the corresponding model has agreed to full testing and certifying as to the accuracy of the model. Most models are simply "validated," which means that appropriate test vectors are developed to expertly validate functional and timing characteristics of a device. These models are then compared to the actual device using a hardware modeler. Validated models tend to be extremely accurate physical models, representing the state-of-the-art in behavioral-model testing. With their behavioral software models, Quadtree Software supports packages by HHB Systems, Gateway Veralog (an analog-simulation company), LSI Logic, Mentor Graphics, Silvar-Lisco, and Valid Logic Systems.

As microprocessor companies make an effort to keep their developments more proprietary, certified models become increasingly harder to develop. As a consequence, other companies, such as Logic Automation, offering validated models, have been better managed to support new developments in VLSI technology. Logic Automation currently supports practically all models of the microprocessors developed by Motorola, Texas Instruments, Intel, National, and Advanced Micro Devices. Logic Automation supports packages generated by Daisy, HHB, GenRad, Mentor Graphics, and Valid Logic Systems.

Quadtree Software models are sold individually at costs between $500 and $5,000. The upper level prices are applicable to the more complex models containing all the latest developments. This includes all 16- and 32-bit microprocessors. Yet, Logic Automation sells the use of their complete library as a single package for $6,000 a year. Additions to the library are made available as they appear without further charge. No penalty exists for discontinuing and subsequently renewing subscriptions. Companies using Logic Automation physical modelers renew their subscription whenever complex physical modeling capabilities are needed. When access is not renewed, logic devices still appear in the user's library and simulation circuit, but they cannot be simulated.

For simulation capability on the PC, ALDEC's Susie package provides logic simulation for a wide range of Intel, Motorola, and T.I. devices. Although this package does not provide sophisticated timing simulation and fault simulation, ALDEC's Susie does provide a means of design verification on the PC platform. This package also interfaces with a number of PC schematic-entry packages, including OrCad, Schema (by Omation), Tango, P-CAD, FutureNet, and Racal-Redac's CAD/CAM version for the PC.

Printed-Circuit-Board Work Systems

Almost all of the large workstation-based companies meet the primary requirements for a PCB system. The larger companies, those meeting at least 80% of all requirements, also provide excellent tools for routing multilayer boards, for creating power and ground planes, and for routing at high speeds.

A few PC-based companies are beginning to compete with the powerful autorouting tools found previously only on large workstations. Table 3, reproduced from EDN News of January 1988, lists and compares PC-based companies that have entered the autorouting arena. Only CAD Software and CALOS route up to 12 layers simultaneously, create power- and ground-planes, and provide back annotation. These two packages also provide design-rule checkers and route boards up to about 3 x 3 ft with approximately 1000 components. CAD Software and CALOS are also the only two companies that provide rip-up and retry autorouting algorithms. PADS Super-router costs about half the price of the CALOS 6000.

Some PC-based packages, such as OrCad and PCAD, have incorporated many features available previously only on mainframe workstations. These features include surface mount, placement of integated circuits (ICs) on top of ICs, and component placement on both sides and use of small outline packages (SOPs). With these packages, the layout engineer can also place copper zones on any layer of any size. Copper zones can be created by using vertical, horizontal, and 45° lines down to 1-mil resolution. Most PC PCB packages include layout error checking for track-to-track, pad-to-track, and pad-to-pad spacing. Most also have more than one routing algorithm, allowing shorter tracks to be placed first and then using a rip-up and retry strategy to route the remaining signals.

Limitations on the PC still exist because of memory limitations. Claims by PC PCB companies of routing boards with thousands of components are often misleading. To compare numbers of components routed by using different PC packages, a baseline must be established. This baseline must include the type of package used (e.g., 14-pin dip) and the total length of tracks placed. The number of components which can be placed depends upon these factors, which in turn rely on the amount of memory addressable by the PCB package.

Another limit caused by the amount of addressable memory is the number of layers which can be routed simultaneously. OrCad plans to add addressing prefixes to allow their package to access expanded or extended memory as a RAMdisk or hard disk. Other PC PCB manufacturers are trying to overcome the handicap of only a small number of libraries being currently available. Many PC CAD manufacturers are making efforts to increase drastically the size of schematic and PCB libraries for their respective packages, particularly for leadless chip carrier (LCC) and SOP parts.

STANDARDS

A number of companies intend to adopt new standards being developed. One recently proposed standard for an operating-system interface has been developed by a group at the Massachusetts Institute of Technology (MIT). A committee was formed that included representatives from large computer-industry companies. This committee agreed to adopt the X-windows format.

Several of the CAD/CAM companies intend to adopt the X-windows format. Included are Racal-Redac, Silvar-Lisco, and Tektronix. (The latter's decision antedates the aforementioned acquisition by Mentor Graphics.) X-windows is intended to become a standard for all workstation operating systems. This standard is being designed to allow a user to move from one platform to another and then pop up an identical window for operating application software. This will provide transparency across the network.

Table 3 — Representatives Personal-Computer-Based PC-Board Autorouters (Introduced Since November 1986)

Manufacturer	Model	Hardware Required	RAM Required (Bytes)	Max Board Size (in.)	Number of Layers Simultaneously Routed	Number of Components Per Board	Power and Ground Planes Created	Back Annotation	Design-Rule Checker	Price and Required Software	Circle Number
ACCEL Technologies 7368 Trade St. San Diego, CA 92121 (619) 695-2000	TANGO route	IBM PC/AT/XT, PS/2	320 K	32 × 19	4	1000	Optional	No	Yes	$495; runs with TANGO-PCB	322
Advanced Microcomputer Systems 2780 SW 14th St. Pompano Beach, FL 33069 (305) 975-9515	NS	NS	512 K	20 × 20	2	NS	Yes	Yes	Yes	$250; required Software NS	323
Bishop Graphics 5388 Sterling Ctr Dr. Westlake Village, CA 91359 (818) 991-2600	NS	IBM PC/AT/XT, 80386, and approved compatibles	1/4 M per 56 sq. in. of routable area	15 × 15	2	NS	No	No	Intrinsic depending on parameters set forth	$2995; runs with schematic capture and layout ($1995); requires AUTOCAD	324
CAD Software Box 1142 Littleton, MA 01460 (817) 486-9521 or 9522	PADS-super-router	IBM AT/XT and 80386-compatible computers	1 M to 2 M	32 × 32	12	900	Yes	Yes	Yes	$4500; runs with PADS-PCB ($975)	325
CALOS 3419 Edison Way Fremont, CA 94538 (415) 657-4430	CALOS 6000	IBM PC/AT 80286 or 80386 with DOS and EGA/VGA graphics	640 K to 4 M	32 × 32	12	950	Yes	Yes	Yes	$11,075 includes schematics, PCB editor, and autorouter	326
Case Technology 2141 Landings Dr. Mountain View, CA 94043 (415) 962-1440	NS	IBM PC/AT 80286 or 80386 or equivalent computer	6 M to 16 M	32 × 32	16	3000	In layout system	In layout system	No	$6500, with 8 M bytes of memory; runs with VANGUARD STELLAR	327
Design Computation Rte. 33, Sherman SO Farmingdale, NJ 07727 (201) 938-6661	DC/Auto-router II version 3	IBM PC/AT/XT, PS/2, or compatible computer	640 K	32 × 32	32	>1000	Yes	No	Yes	$2450; runs with draftsman-EE editor with routing tools ($975	328
OMATION 1210 E. Campbell Rd. Suite 100 Richardson, TX 75081 (800) 553-9119	SCHEMA-route	IBM PC/AT/XT and 80386; EGA color mouse, hard disk	640 K	32 × 32	2	400 equivalent ICs	Yes	Yes	Yes	$750; runs with SCHEMA PCB ($975)	329
ORCAD Systems 1049 SW Baseline St. Suite 500 Hillsboro, OR 97123 (503) 640-5007	ORCAD/PCB auto/manual router	IBM PC/AT/XT, PS/2, or compatible computer graphics card	640 K	32 × 32	2	As many as 2500 pins	No	No	Yes	$1495; runs with ORCAD PCB	330
Personal CAD Systems 1290 Parkmoor Ave. San Jose, CA 95126 (408) 971-1300	Master designer 386	IBM PC/AT or compatible computer (80286 or 80386); expanded memory	640 K	60 × 60	32	As many as 1300	No	Yes	Yes	$16,980 includes complete design system	331
Visionics 343 Gilbraiter Dr. Sunnyvale, CA 94089 (406) 745-1561	EE designer auto-router II	IBM PC/AT/XT, PS/2; and compatible computers	640 K	149 sq. in.	2	1000	Yes	Yes	Yes	$1495; runs with EE designer II	332
WINTEK Corp. 1801 South St. Lafayette, IN 47904 (800) 742-6809; IN (317) 742-8428	NS	IBM PC/AT/XT or PS/2	512 K	10 × 16	2	As many as 5120 pins (connections)	No	No	Yes	$895 includes smartwork PC-board package	333

NS Not specified

Racal-Redac has decided to adopt X-windows for their CAE system. They made a further decision to include it with other industry standards such as NFS, a network file-format standard, and Structured Query Language (SQL).

As a company required to interface to many systems with its testing devices, Tektronix has adopted all of the industry standards, NFS, SQL, and planned to adopt the X-windows standard. Hewlett-Packard has adopted the Electronic Design Interface Format (EDIF) for file exchange. The latter company may be slow to adopt other standards since, to date, the choice of the company has been a proprietary, closed-architecture system.

It is anticipated that such companies as Computer Vision and Mentor Graphics will make every effort to keep their systems closed and proprietary. This probably means that it will be some time before industry standards are more widely adopted, in particular X-windows.

TESTING INTERFACES

The most prevalent testing interface is the one developed by Test System Strategies, Inc. (TSSI). This company was formed as an offshoot of Tektronix. Its founders decided that an industry standard should exist for interfacing with testing equipment to allow for board testing in completing the design and simulation of hardware.

Most large companies have adopted the TSSI interface for integration to testing equipment. These companies include Computer Vision, G.E. Calma, HHB, GenRad, Mentor Graphics, Racal-Redac, Silvar-Lisco, Tektronix, and Teradyne. This provides an interface to Tektronix's powerful Digital Analysis System (DAS 9200). The DAS 9200 provides prototype and limited production-board testing capabilities as well as board software debugging and analysis.

DOCUMENTATION

Documentation requirements normally consume a great deal of the engineer's time. They include such items as reports, proposals, manuals, and system specifications. In designing digital hardware, documentation can include incremental design annotations for each stage of a design, design annotations for possible trouble-shooting, annotations specifying connections to a larger system, and internal design annotations.

Documentation packages that allow an engineer to expediently document design decisions and their effects on board design are necessary in a CAE system. The first package to allow a designer to incorporate schematics and text was developed by Interleaf. This has been the standard such package for comparison for documentation capability. It provides tremendous capability in manipulating text and schematics to yield presentation-quality documentation. This advanced electronic publishing system runs on the SUN, Apollo, Apple, Digital, and IBM workstations.

In the interim since Interleaf developed their documentation package, another company, Ventura, has also marketed a comparable documentation package. Ventura was subsequently acquired by the Xerox Corporation who now markets the Ventura publication package. These packages offer tremendous capabilities for integrating schematics, waveforms, and text supplying the additional documentation needs of a design engineer.

PROPOSED SOLUTIONS

Proposed Solution Number One

The first solution recommended for CAD/CAM development is a PC-based system making use of the OrCad System schematic entry and PCB packages, the HHB CADAT logic simulator, and Logic Automation physical modelers. The inclusion of HHB CADAT also permits interfacing to the Interleaf documentation package. The overall system would cost about $32,000. The Interleaf package would cost an additional $5,000.

This solution provides the interfaces needed to develop an integrated, turnkey system for CAE. OrCad meets more of the schematic entry requirements than any other package available for operating on the PC, 89% of such requirements. The solution is one of the most versatile and user-friendly packages available. OrCad's package is available at $3,080. NRL's Ships EW Branch already has several of OrCad's schematic-entry packages.

To repeat some of the factors that led to this solution: Of the six possible sources of logic simulation identified as supporting all requirements to some degree, only four of these have kept up with new IC and VLSI developments. Of this group, only the CADAT package offers more than one interface, and a version is available for PC-based systems. The CADAT package, because of its interfacing and state-of-the-art logic simulation capabilities, is the most widely used logic simulator at this time. CADAT is also the only logic simulator providing these capabilities for less than $200,000, as DASH-CADAT PLUS.

Two companies that specialize in physical modeling also interface to CADAT to produce even more modeling capability for complex microprocessor devices. These companies are Quadtree Software and Logic Automation. The latter is the only source of physical models for the most recent Intel, Motorola, and Texas Instruments microprocessors.

CADAT is one of only two logic simulators that explicitly provide concurrent fault simulation. This feature saves considerable time when testing multiple-serial fault paths.

OrCads PCB package is adequate for boards with up to approximately 200 14-pin dip-type packages. Copper zones of any size can be created on any layer down to 1-mil resolution manually and 5-mil resolution with autorouting. OrCad's package does not back-annotate gate or pin swap. Instead, OrCad allows the designer to recompile a schematic which has already been laid out. Any changes in the design can be rerouted without affecting routed unchanged connections. OrCad has several routing algorithms, including a 90° strategy, a no-via strategy, a rip-up option, and an optimizer. The rip-up option reprioritizes routes by accommodating any unrouted signals directly and ripping up any previously routed signals in the path. The optimizer attempts to reduce vias and tracks.

In summary, this PC-based solution will allow quick access to the hardware necessary to support the software. It also provides an easy means for transfering files to other PCs. An 80286-based PC with a 130-megabyte hard disk and 16 megabytes of memory is recommended. This configuration meets all necessary installation requirements and still allows a significant reserve of memory for simulation and CB-design computations, and it allows sufficient storage of design files along with applicable software.

Proposed Solution Number Two

The second CAD/CAM system solution recommended is that by Racal-Redac and HHB's Visula-CADAT version on a SUN platform. This system costs $189,500 with the inclusion of Interleaf's $5,000 documentation package.

Racal-Redac meets 95% of the stated requirements, more than any other system after Mentor Graphics' acquisition of the Tektronix CAE division. Not only is this an exceptionally powerful CAD/CAM system, but it is also well-integrated and user-friendly. The company has developed a broad base of customers, including many in the military. Two systems are in place at NRL, and the company services the Metropolitan Washington area from a Northern Virginia location.

Racal-Redac has already adopted applicable industry-wide standards, including NFS and SQL. It has agreed to the adoption of X-windows. When these standards are used with platforms such as the Apollo, VAX and SUN, tremendous flexibility becomes available to manipulate files and interface with additional equipment.

Through the CADAT interface a designer has a direct connection to testing equipment utilizing the TSSI format. Also, standard ASCII files are created; this allows a designer an easy access to upload and download program code used to develop a system.

Configuration control, as used in the military aerospace communities, is a part of the system. This results in design reliability, availability of MIL-SPEC versions of parts, and the addition of controls to ensure proper documentation.

Through the Interleaf documentation package a designer can easily integrate text with schematics. Accuracy is ensured by denying access for editing a schematic after the documentation package has been entered. Such editing is restricted to the original schematic rather than a documentation copy.

The benefits of CADAT that have been covered in Solution No. 1 are equally available in this solution. These also include plans by HHB to enlarge its analog simulation capabilities by using the SUN platform and Visula-CADAT. Should analog simulation beyond simple components (such as pull-up resistors) be desired in the future, this system would be the best solution. It would then allow concurrent simulation of analog and digital components on a board or comparisons of "equivalent" analog and digital circuitry.

Proposed Solution Number Three

The system described in this solution is what would be offered by Teradyne for about $249,300 with the VAXStation 3520 or 3540 workstations. The system would have superb capability for schematic entry, logic simulation, and PCB design. Teradyne's recent acquisition of Case Technology gives the former access to one of the leading schematic-entry and PCB-design packages. A fully-integrated operating environment between the schematic-entry package and LASAR has now been effected.

As already noted in some detail, the Case Technology package is extremely user-friendly and versatile. Placement and routing software is interactive to provide both manual and automatic placement and routing of isolated areas or of an entire board layout, including multilayered boards. Tremendous flexibility exists to define wire widths and pad sizes for soldering.

Not only does Teradyne allow min/typ/max timing, but it will also take into account such circuit properties as gates that tend to track one another and the common origination of signals. LASAR

provides detailed hazard reports that completely describe any possible design problem and suggest the likely causes of the hazard. With the use of Teradyne's hazard reports, a designer has greater flexibility in logic simulation to determine the sources of glitches and to decide whether they will affect the actual board operation. Serial and concurrent fault-simulation capabilities are provided along with test-pattern generation for board verification.

Teradyne's recent acquisition of AIDA added more board-testing capability. From this move integretion of logic simulation and board testing has developed. This integration has made it possible to input additional information to the board-testing equipment to test for current loading and power-source arcing.

Running on the VAX platform provides a standard and familiar operating-system environment. This also provides more powerful operating system tools and easy transfer of files from other VAX systems, including those based on mainframes. When compared to using the PC platform, the use of this platform greatly reduces running time. Comparisons of compute time for running Teradyne's LASAR on the SUN vs running on the VAX, show the VAX VUP (VAX unit of performance) as having more computational power than the SUN MIP (millions of instructions per second) for this particular application software.

The Teradyne system can be purchased for $249,300. This price includes hardware modeling for the Intel 20826, Motorola 68000 and 68020, and Texas Instrument TMS32020 and TMS320C25. It appears to be more efficient and less costly for NRL to purchase the VAXStation from Teradyne than from Digital Equipment Corporation under the GSA Schedule. This would allow acquiring the Teradyne system for $180,300. $83,800 of this would be for schematic design, logic, and fault simulation, plus the PCB layout with design-rule checker. The remaining $96,500 would cover the cost of the hardware modeling subsystem.

In an environment heavily geared toward production, many board-design problems may go undiscovered until manufacturing is completed and mass production has begun. The Teradyne system would preclude most of these problems and save countless manhours of work. This solution offers the most comprehensive set of logic- and fault-simulation capabilities while providing flexibility in a CAE system. In such an environment or one where design reliability is critical, this system would be the number-one recommended system.

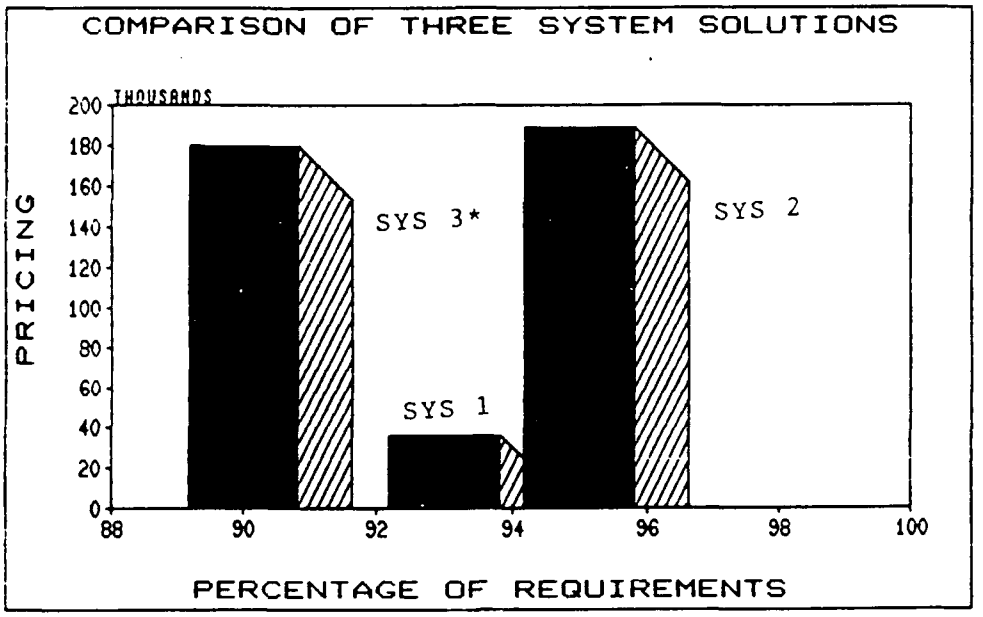
PRICE/PERFORMANCE FOR THREE PROPOSED SYSTEM SOLUTIONS

Figure 1 graphs the comparative advantages of each of the three proposed systems when pricing is compared with the percentage of requirements fulfilled. In the graph, System No. 1 consists of OrCad and HHB Systems. System No. 2 consists of Racal-HHB, and System No. 3 of Teradyne.

SYSTEM MAINTENANCE

When any new system is purchased, time and effort are required for setting up the system. This effort includes the installation of software on the chosen platform, the development of directories for parts and symbol libraries, and a minimum amount of training for the users. Actual users must be able to produce results with minimal effort. Initial training and system management and long-term maintenance are therefore vital to the effectiveness of the CAE system.

To achieve effective system maintenance, an individual must be designated as a central point of contact to interface with the appropriate vendor(s) and to develop prompt vendor service and support. This point of contact will make all repair calls for both hardware and software. In the absence of the



*System No. 3 has added simulation and testing capabilities beyond requirements.

Fig. 1 — Graph of comparative system advantages

primary point of contact, one or two alternates should be named to place service calls. This arrangement will assure the proper functioning of the CAD/CAM system and its maximum use and benefits.

RESULTS OF EVALUATION OF TERADYNE'S CAD/CAM SYSTEM

Background

In the period of 5 to 7 June, 1989, Code 5740 at NRL conducted an evaluation of Teradyne's Electrical CAD/CAM System. This was made possible by that company by loaning a system for the evaluation. Appropriate engineering support was also provided.

After this brief period at NRL, Teradyne continued the work at their headquarters. This phase of support addressed areas that, because of lack of enough time, could not be appropriately evaluated in the NRL phase.

Goals of the Evaluation

To evaluate the Teradyne system, a set of goals was compiled:

- Follow the simulation process through step-by-step. (Examine accuracy and ease-of-use.)
- Intuitively analyze LASAR's process of integrating program code, memory, and programmable logic into the simulation process.
- Test the input of the CASE netlist generated by OrCad.
- Compare the PCB layout and routing between PadsPCB and CASE for a simple circuit.

- Test both layout and routing for a complex multilayer board.
- Examine LASAR's ties to analog simulators (in particular to Analog Design Tool's simulator) and examine the front-end simulation of DACs.
- Analyze LASAR' capability as a tool for accomplishing reverse engineering.

These evaluation goals were also made available to Teradyne so that they could demonstrate the ability of their system in accomplishing these goals. The successful accomplishment of the goals was the criterion for determining whether the Teradyne system met the CAD/CAM requirements of NRL Code 5740.

DETAILED DISCUSSION OF GOALS

Goal Number One

This goal was designed to determine how much time is required for a relative novice designer to learn Teradyne's CAD/CAM system and determine whether such a person might learn the system on his/her own. Two approaches were taken.

In the first approach, a Teradyne applications engineer stepped through the design and simulation process with a schematic supplied by NRL. During this process, NRL personnel received hands-on practice with the system. After about four hours, the flow of the design process, the most commonly used commands, and the system menu started to become familiar to the participants. It became evident that a designer could successfully bring up the system and take a design through schematic entry, the electrical design rules checker, simulation, and PCB layout with minimal reference to the manuals. It was also found that Teradyne's menu supplied one- and two-keystroke easily executed commands. It was learned that the interface was identical regardless of whether the user was entering a schematic, running through a simulation, or creating a PCB layout.

For the second approach, a second copy of the system was loaded on a personal computer to allow a designer unfamiliar with the system to learn with only the manuals as a guide. The manuals were easy to follow. They contained tutorials for each procedure. The particular designer participating in this activity was a student summer employee who spent about one week in learning the system completely. The student also spent time learning OrCad. Both the OrCad and CASE systems were easy to use; the latter required more time because it provides more capability than the former.

Goal Number Two

This goal was designed to "see" the Teradyne system in action, dynamically changing simulation results with input-circuit changes. The objective was to verify that the system would accomplish the claims of the promotional literature and that simulation results would agree with the actual hardware results.

For this procedure, NRL provided a schematic of an 80286 circuit containing 59 ICs and 89 components. The schematic was taken from a board that had already been wire-wrapped and tested. The board contained 64K of ROM and 16K of RAM; it also contained 3 PALs. NRL provided code for a program initializing a counter/timer and USART. It then outputs a message to a monitor through RS232 and allows commands to be input to examine or modify memory, input and output to ports, examine registers, set breakpoints, and execute code.

This schematic was entered into the CASE VANGUARD portion of the system; it occupied three E-size drawings. A library symbol was created for Intel's 82389 chip, a 149-pin PGA device. The simulator imports PAL code by using PALGEN or Circuit Maker, with JEDEC files supplied. (Circuit Maker packages the fuse-map files into PAL models.)

A Teradyne engineer wrote a program to automatically load the NRL PAL files that had been created by using PALASM. For the ROM model, Teradyne's LASAR simulator accepts Intel HEX code. The schematic was compiled. The process of compilation identified problems in the circuit entry. After making corrections and recompiling, the simulation process was started.

The first simulation run produced an overflow error in the ROM model. A block of code filled with Fs after the program code overflowed past the 80286 start address, FFFF0, where the 80286 automatically initializes. The block of Fs was removed from the simulation code, and the 80286 start address was forced to FFFF0. The simulation was then rerun with the 80286 finding the initial jump instruction at FFFF0. This proved that the PAL model was functioning correctly and had been loaded correctly with the engineer's program. However, the 80286 did not jump to the correct program code. Apparently, the ROM model was not functioning correctly.

After reviewing the steps taken to load the ROM code into the simulator and when several runs had been made, Teradyne agreed to look more closely at the ROM model simulation at corporate headquarters. After close examination of the ROM code and the program loading the code into the simulator, the problem was identified. The checksum was treated as executable code by the program loading the ROM code. This explained the overflow error in the ROM model and the simulation not finding the correct code after the initial-jump instruction. Teradyne successfully ran the revised simulation and provided hard copies of the results. Figures 2 through 7 show samples of these results.

The results were identical with results seen on the logic analyzer with the actual hardware. The simulation duplicated results of the communication between the various components in the actual hardware.

Goal Number Three

This goal was included to determine with how much ease simulations might be run and PCB layouts might be made for schematics already entered under OrCad. This package has been used extensively within Code 5740 for the production of schematics. Ninty-five per cent of these schematics have not been used to create printed-circuit boards. The requirement exists to transfer connectivity information to the Teradyne system on a workstation to simulate, place components, and route.

To address this requirement, a schematic entered under OrCad was used to generate OrCad's version of Teradyne's CASE netlist. Figure 8 shows a sample from the netlist that was produced in this phase.

The netlist illustrated is, indeed, very similar to the CASE netlist. However, OrCad failed to put the name of the component part at the beginning of the first line of the component description. Instead, the component part name was placed under the shape property. All connectivity information is, however, provided in the netlist. By examining the netlist exclusively, a designer can edit it and generate a valid CASE netlist. To change the netlist, the designer must move the component name to the beginning of the line where it is contained and add the component shape to the netlist.

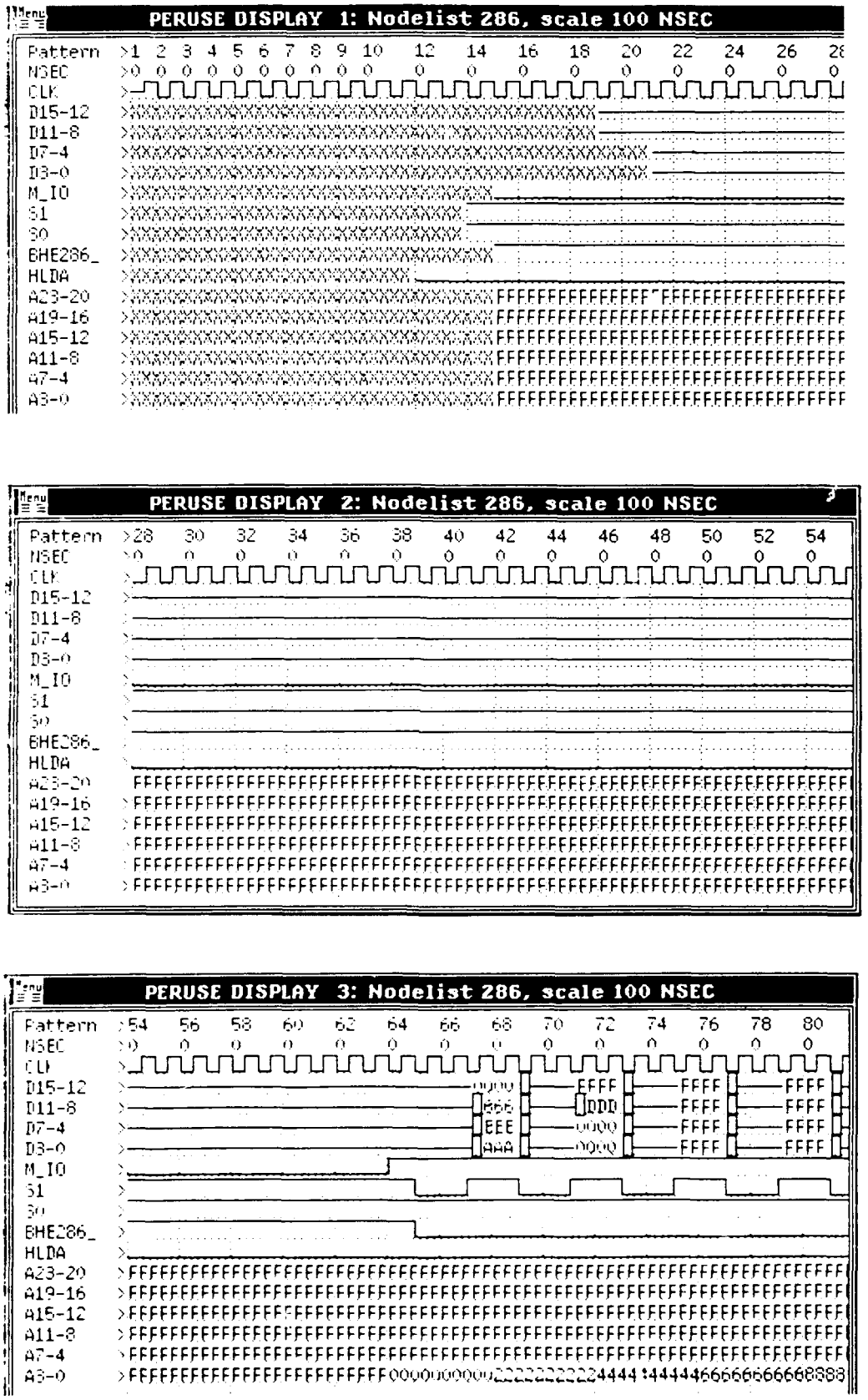


Fig. 2 — Demonstration peruse displays 1, 2, and 3

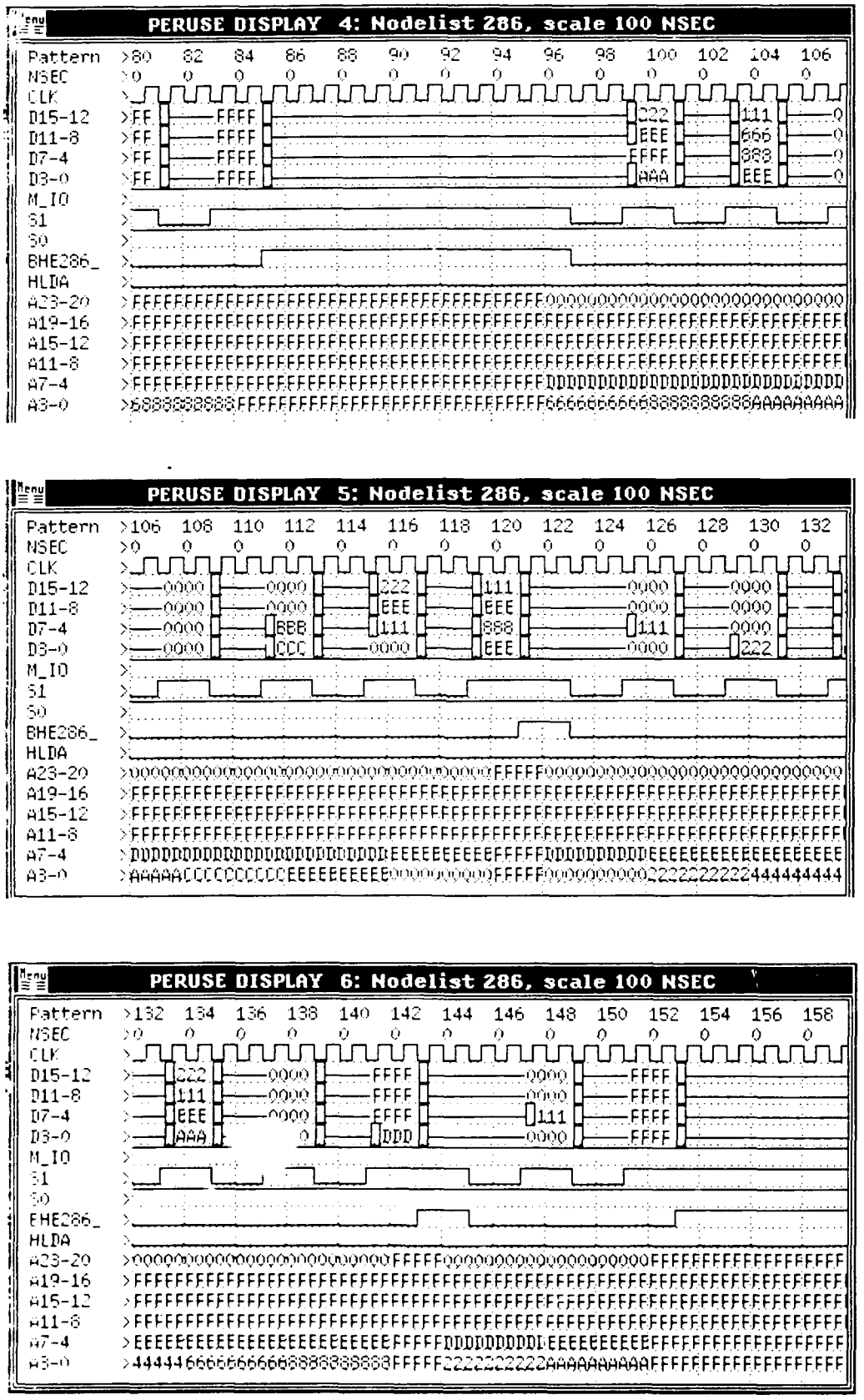


Fig. 3 — Demonstration peruse displays 4, 5, and 6

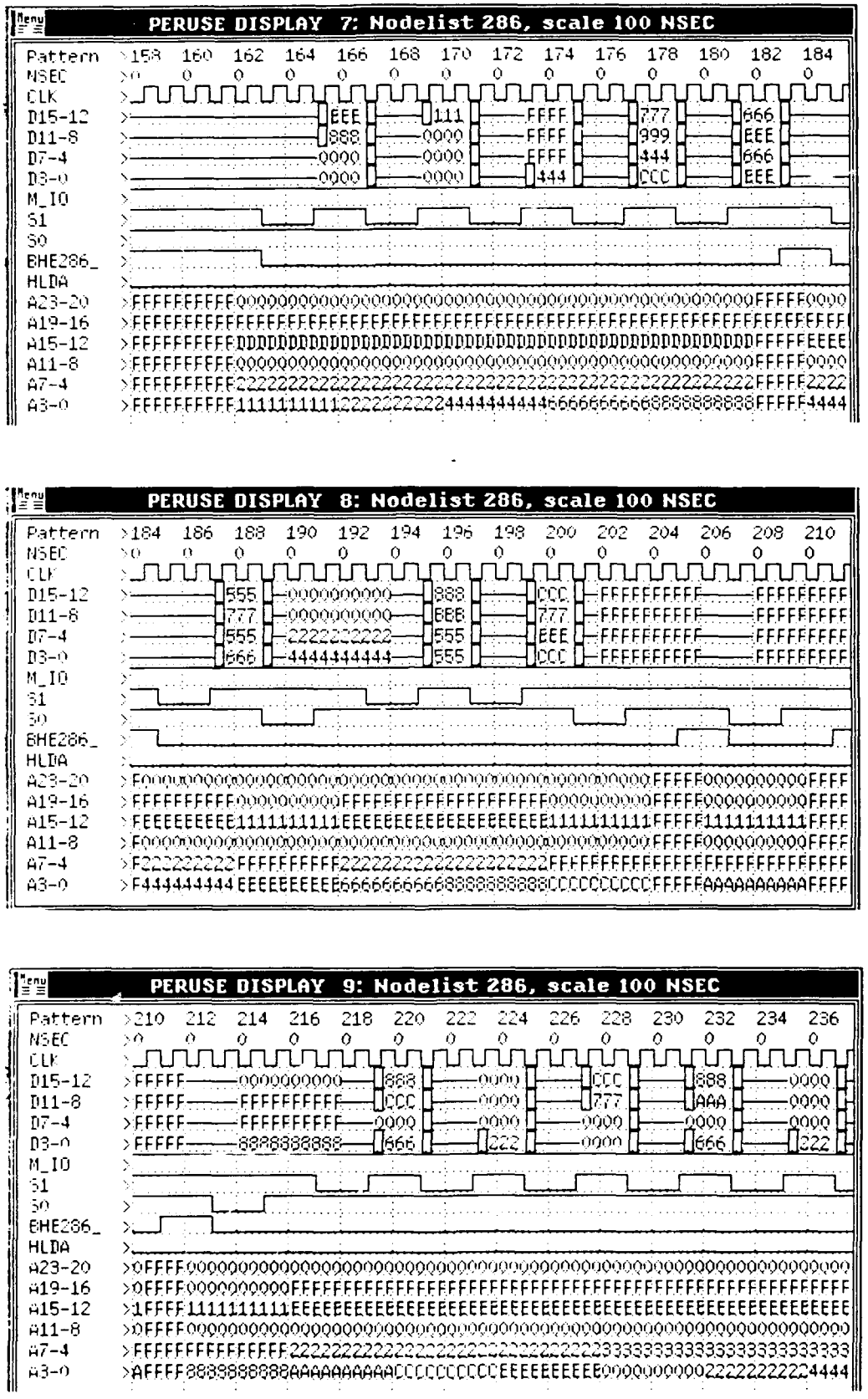


Fig. 4 — Demonstration peruse displays 7, 8, and 9

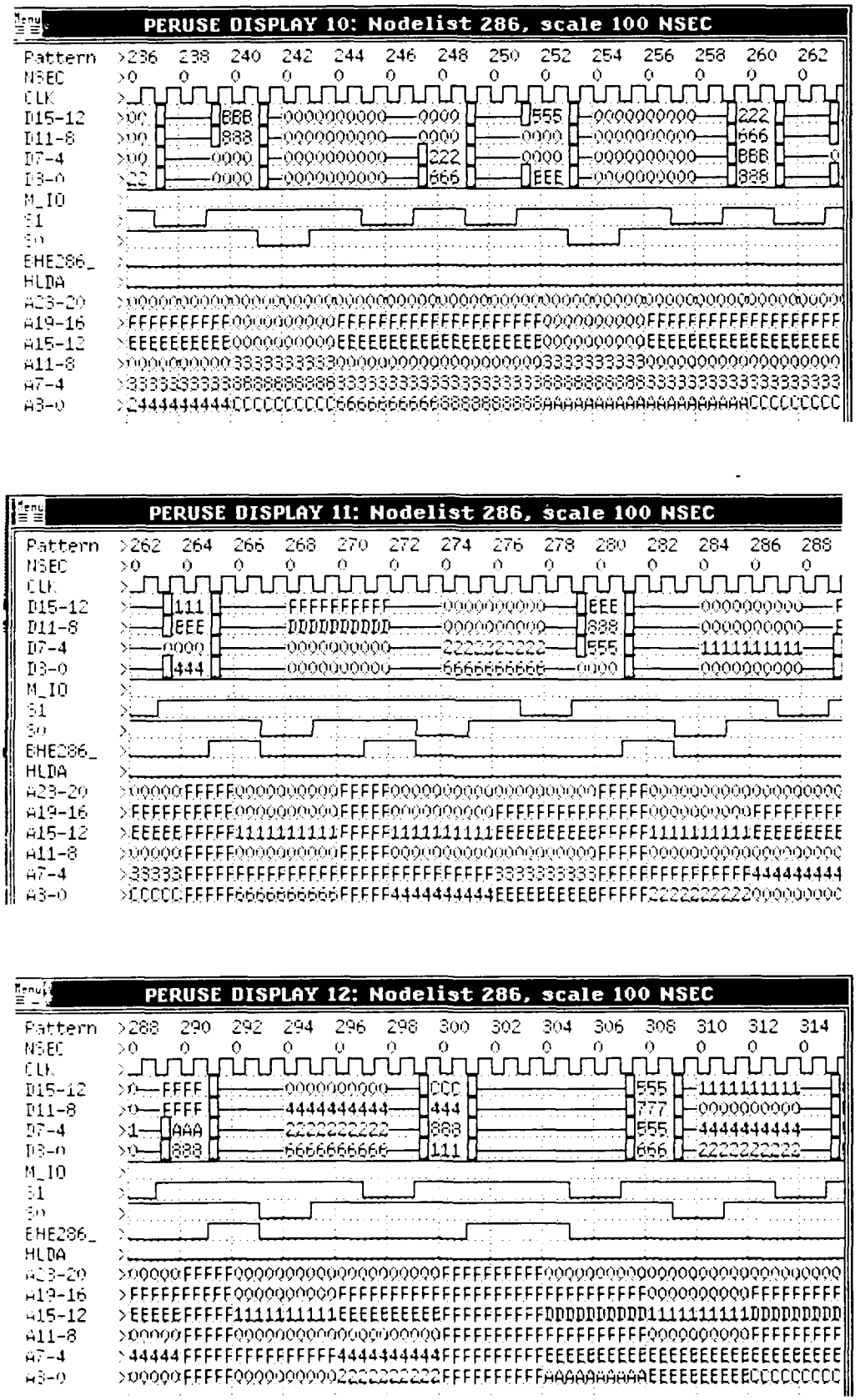


Fig. 5 — Demonstration peruse displays 10, 11, and 12

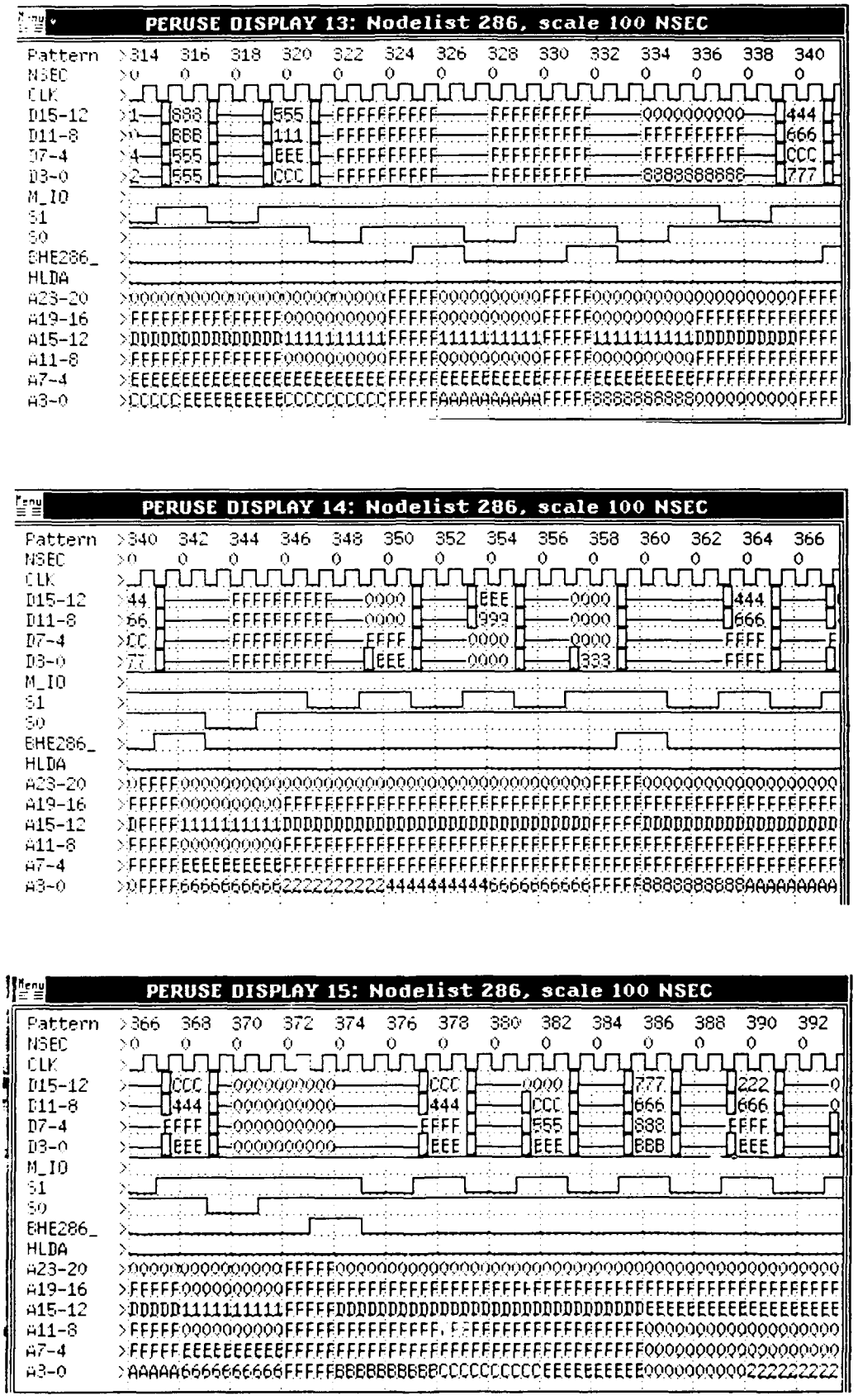


Fig. 6 — Demonstration peruse displays 13, 14, and 15

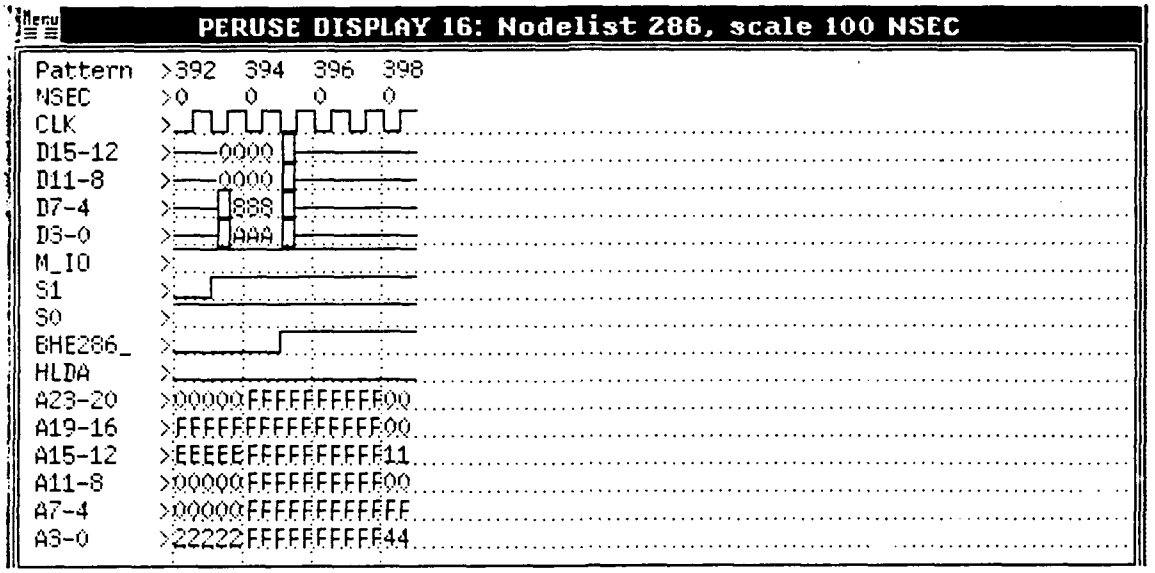


Fig. 7 — Demonstration peruse display 16

```
[SIZE=1;TIMES=1;LOC=(U83 );FLOC=U83;SHAPE=54ALS273]
1=VCC/A14;
2=ICU3;
3=DATA_BUS0;
4=DATA_BUS1;
5=ICU1;
6=ICU2;
7=DATA_BUS2;
8=DATA_BUS3;
9=ICU3;
10=DGND;
11=X00181;
12=ICU4;
13=DATA_BUS4;
14=DATA_BUS5;
```

Fig. 8 — A sample for the netlist

Goal Number Four

To achieve this goal, a designer experienced with the PadsPCB package became familiar with the CASE VANGUARD PCB package. The designer then found that both packages produced standard Gerber photoplot files and that both packages can handle analog parts along with digital components.

CASE's usefulness was examined for placing copper for shielding hybrid boards, for irregular shape filling, for providing shields and an overflash on unconnected pins on a multilayer board, and for placing off-grid and in meters down to thousandth fractions. The test was successful.

CASE's autoplacement program provides a filter to control the order of placement, allowing larger ICs and those ICs with more signals connected to be placed first. The CASE VANGUARD

package was also more automated since all the needed information is passed directly from the schematic capture program.

Goal Number Five

This goal was designed to test the ability of the Teradyne system to add multiple power and signal planes and to route a multilayer board. Also tested was the ability to create varying pad sizes for pins and to produce artwork for both surface-mount technology and Gerber photoplotting.

Among the items provided by Teradyne for the test was a copy of the schematic entry and PCB layout system for the PC. The complex schematic used for Goal No. 2 was also used for Goal No. 5.

A 135-pin 80386 PGA layout model was modified to a 149-pin PGA layout model for the 82389 device. All similar logic gates were automatically packaged together with the same reference designators. The components were manually placed optimally (with understanding of the purpose of the circuit). Analog and clock lines were manually routed also. Because of circuit complexity, 8 megabytes of extended memory were needed for autorouting. The layout, with manually routed signals, was sent to Teradyne for routing to be completed with the autorouter. Artwork was produced for an 8-layer board comprising four signal layers, one GND layer, one +5 Vdc layer, one analog GND layer, and one layer providing ± 12 Vdc.

Goal Number Six

The importance of this goal arises from the fact that a substantial amount of analog-related design and testing is done by Code 5740. In support of this work, a contract is being negotiated for an analog design and simulation system. A system produced by Analog Design Tools (ADT) proved to be one of two systems with extensive capability. This company also agreed to contract out work to recognized experts in vacuum tubes and relays to provide reliable models of such vintage 1920 devices. Another reason for seeking an interface with ADT is their unique menu-driven interface, an interface not available from any other simulation package.

With the CASE VANGUARD schematic entry, a designer can build circuits that include both analog and digital parts. The system provides a shell around the schematic entry portion. CASE allows the designer to run SPICE and PSPICE directly from its menu. Because ADT is based on the SPICE simulator developed at the University of California at Berkeley, ADT's package can also be run from the CASE menu. Digital input to DAC devices is provided through the CASE system, and analog signals to A/Ds are, stepwise, linearly integrated to provide the digital information back to CASE after analog simulation.

Also, Teradyne already has contracts with customers that are running both analog and digital simulations through the use of the digital simulation capability of the Teradyne system, mated with ADT's analog simulation system. The CASE VANGUARD schematic entry is the interface for this combination.

Goal Number Seven

The schematic used in this goal was the one used for Goal No. 3. Two digital interfaces were used in the circuit. One of these used the Multibus II standard interface. Protocol for this interface is handled by Intel's Message Passing Coprocessor (MPC) chip, the 82389, a 149-pin device. For simulation purposes, Teradyne uses hardware modeling for complex microprocessor parts; actual parts are used in the hardware modeler.

The hardware modeler is run on a VAXStation other than the Model 3100 supplied by Teradyne for the evaluation. The modeler interfaces through either the Q-Bus or through the Unibus. There is no bus structure in the 3100; it has an SCSI port. The modeler is nonportable. To watch a simulation with the 82389 or another complex microprocessor requires continuing the evaluation at Teradyne corporate headquarters. In the actual test, an alternate approach was taken.

Teradyne had both software and hardware models of Intel's 80286 microprocessor. The company simulated this circuit with the hardware modeler at their headquarters. The hardware model ran exactly as the software model. It was concluded that all software overhead for the hardware models was transparently executed with respect to the circuit simulation. Thus, by using hardware modeling for any complex device, an accurate simulation displaying the complex signal-timing patterns could be obtained.

Goal Number Eight

This goal was designed to examine the ability of a designer to determine functionality from examining outputs of a circuit with known inputs. It was established that the system's hardware modeler is ideally suited for this purpose. Any existing digital hardware can be mounted on the hardware modeler. Leads can then be connected to all inputs and outputs. Inputs can be generated from the computer, and outputs can be monitored on the timing diagram. Additional tools exist for generating multiple input patterns automatically. This considerably reduces the time required to generate test results.

Figure 9 is a diagram of the counter/timer circuit that was used to test the acheivement of this goal. The circuit was entered into the CASE schematic entry system. Inputs were then applied to the circuit to test how well the goal might be realized in an individual circuit.

Figures 10 through 13 show the hard copy simulation results. One input causes the outputs to sequence through a counting pattern at the same rate as the second input. By assuming that this circuit was actual hardware and that the hardware could be broken down into the three parts identified with blocks on the circuit, a second set of simulations was run with a subset of the circuit. The set of hard copies indicates how, by using this approach, a large amount of information can be accumulated with respect to circuit functionality.

Additional Results of the Evaluation

Along with the information derived and discussed in the preceding paragraphs, the following features were found to be valuable assets in the schematic design process:

- Teradyne's Electrical Rule Checker (ERC) provided error and warning messages about real circuit design problems that would have led to unreliable operation. The ERC identified problems with:
  - Mixing technologies,
  - Multiple outputs, tied together without tri-state outputs,
  - Low driving current,
  - Open collector outputs, tied to signals driving both to VCC and GND,
  - Excessive capacitance on lines,
  - Signals without sources,
  - Signals without input loading.
- Teradyne's toll-free customer support was able to provide ready answers to questions on software operation. Directions were given on where to locate operations on the menu, what quick-and-easy commands were available without the menu, and clarification of differences encountered when using different operating systems.

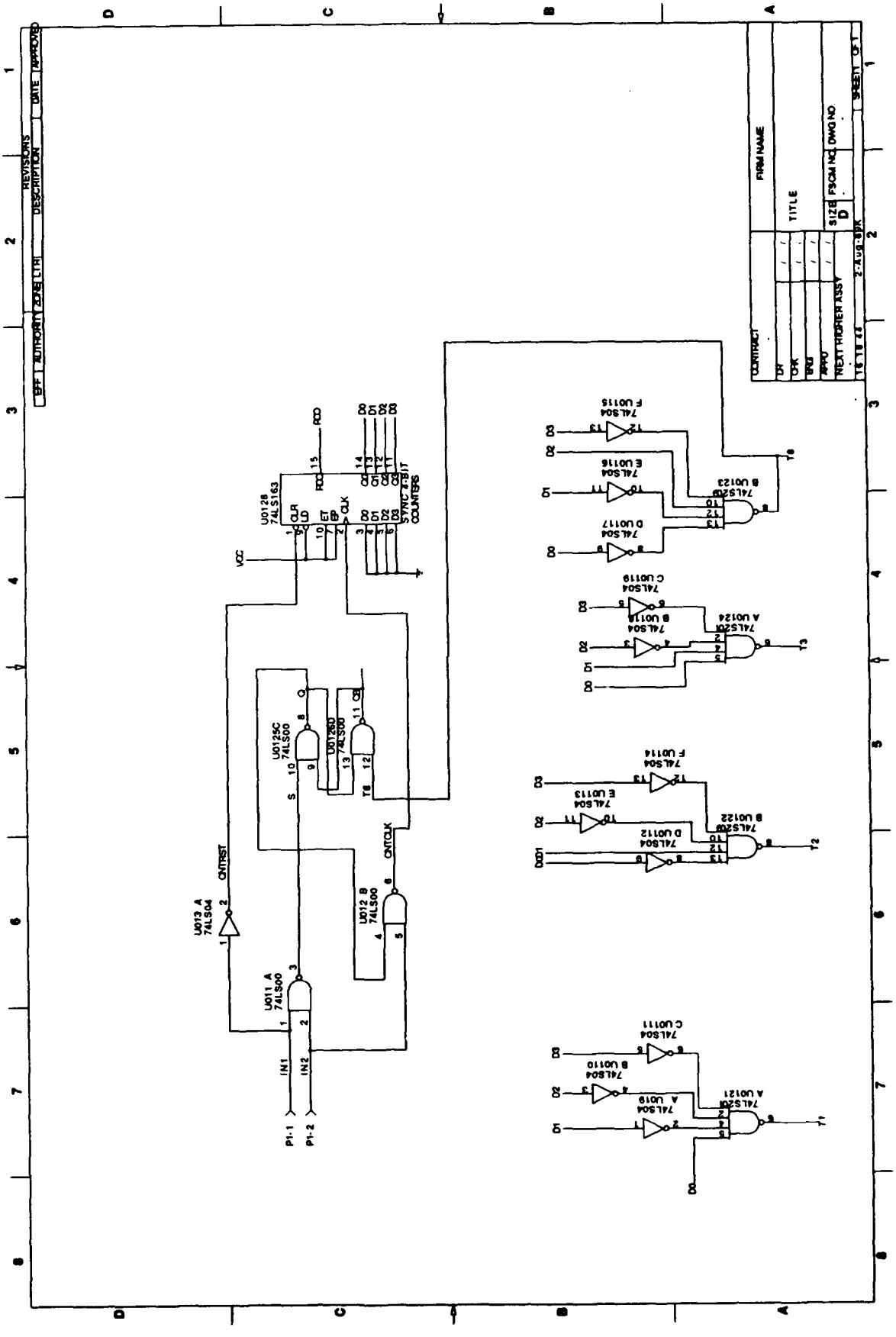


Fig. 9 — Diagram of counter/timer (C/T) circuit

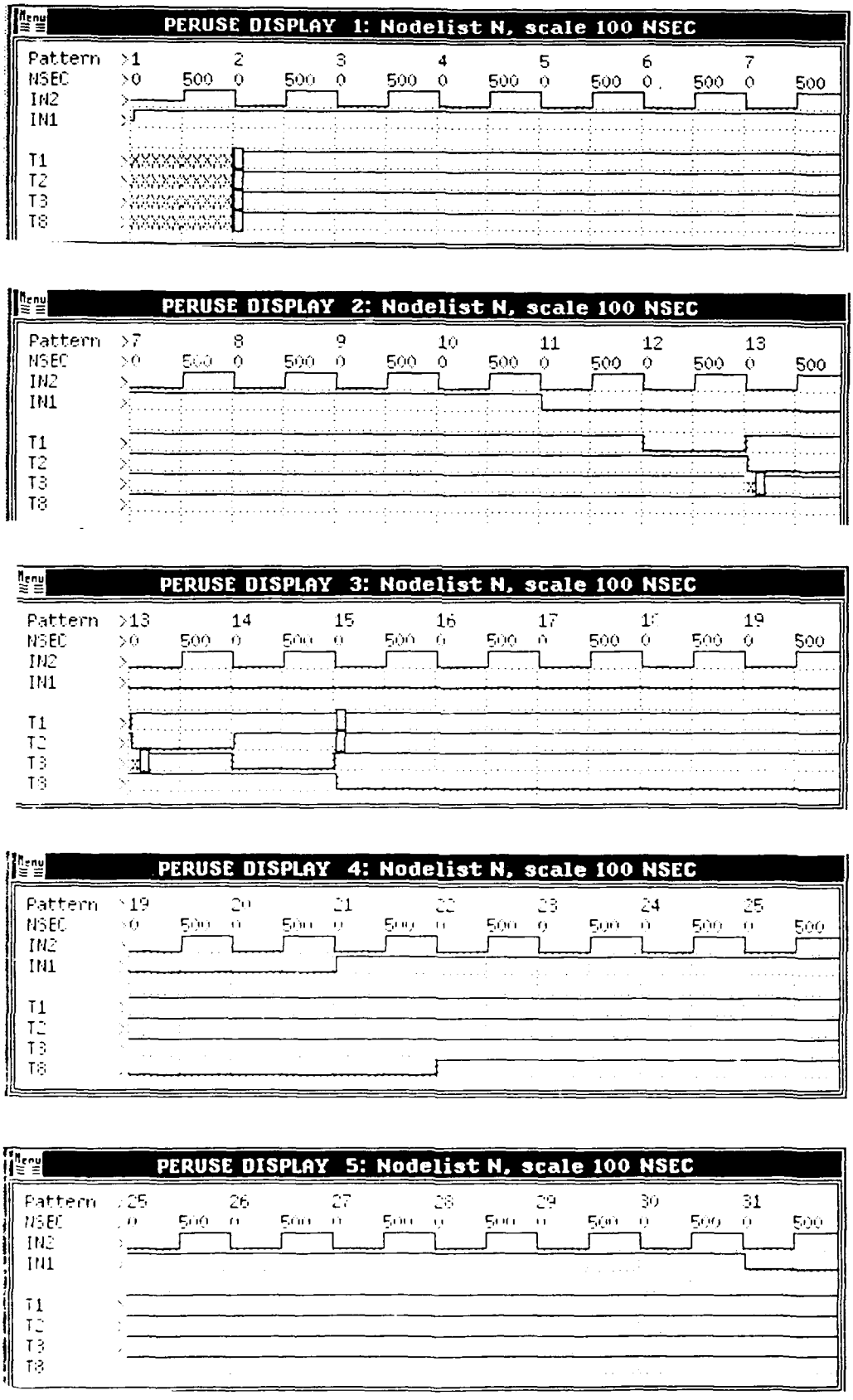
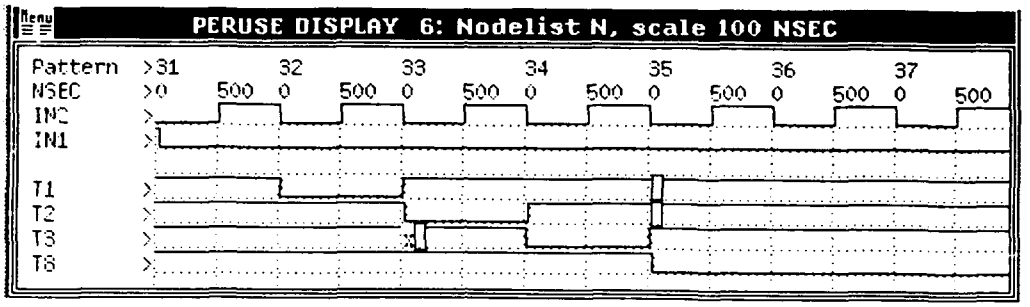
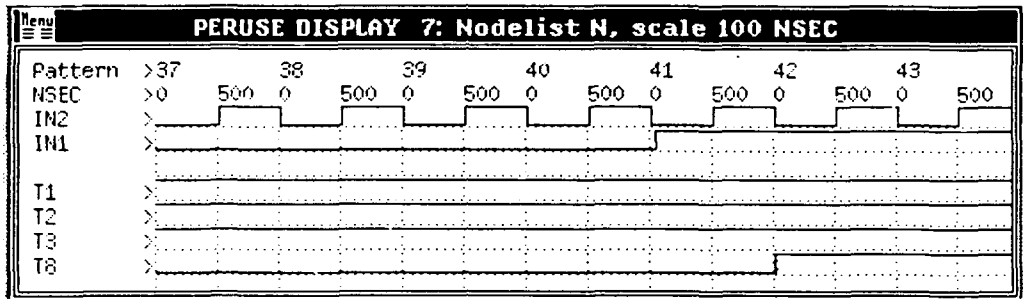
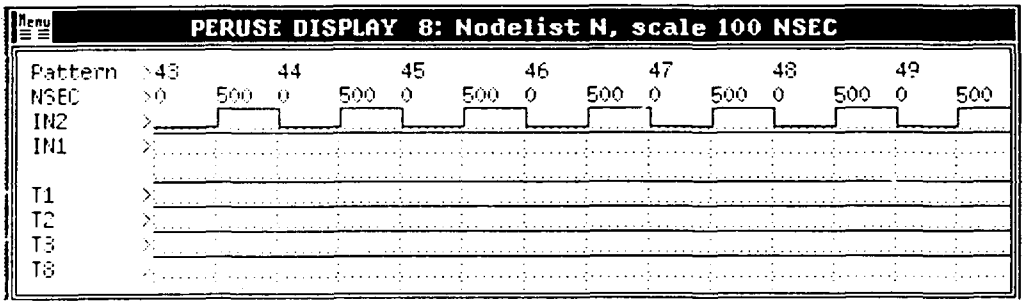
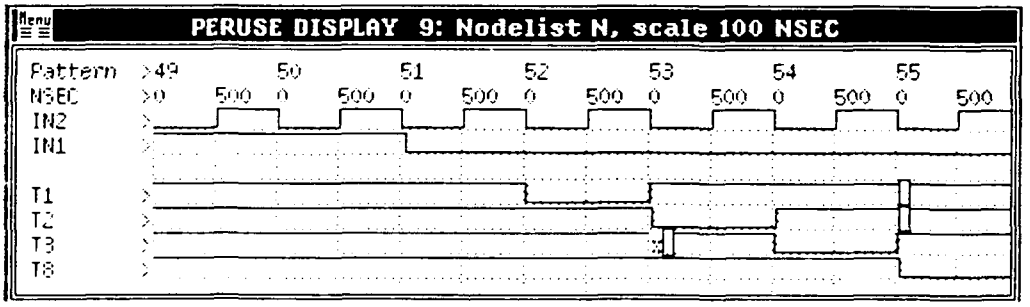


Fig. 10 — C/T peruse displays 1, 2, 3, 4, and 5









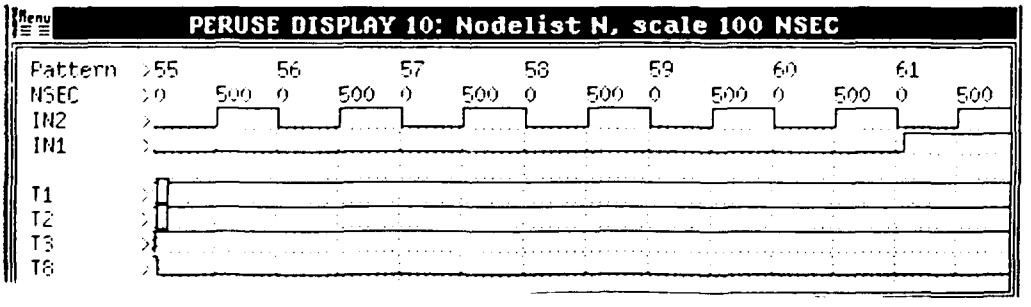


Fig. 11 — C/T peruse displays 6, 7, 8, 9, and 10

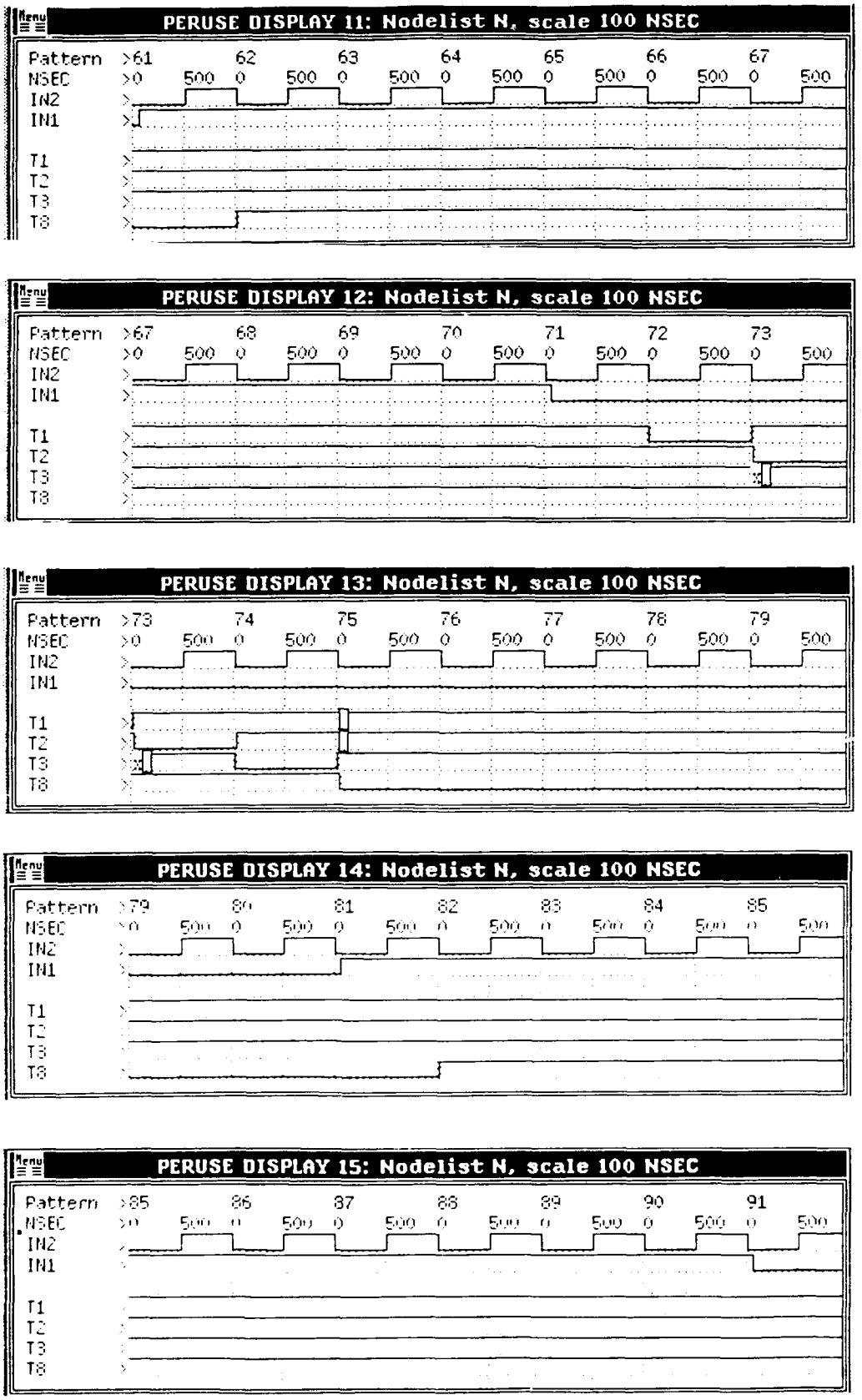


Fig. 12 — C/T peruse displays 11, 12, 13, 14, and 15

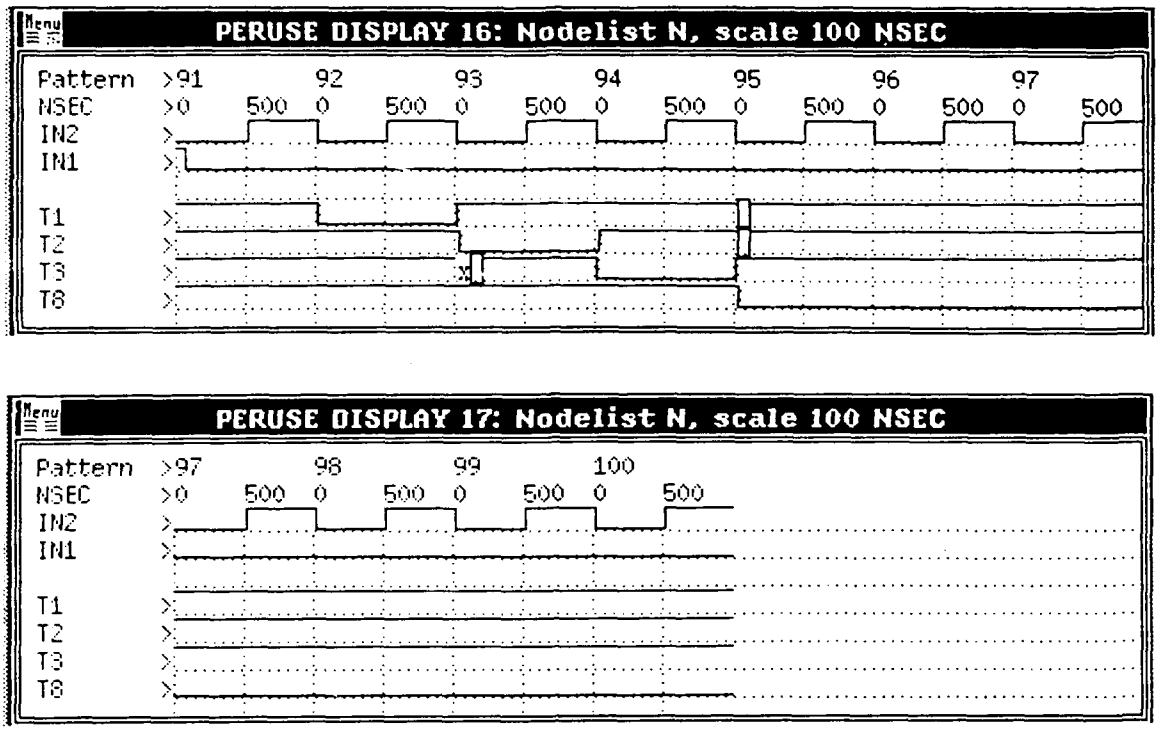


Fig. 13 — C/T peruse displays 16 and 17

SUMMARY

The evaluation required several goals to be accomplished in a short period of time. These goals determined the applicability of the Teradyne system to several different projects. NRL Code 5740 was able to determine that the Teradyne system could meet all foreseeable requirements for CAD/CAM design and provide additional capability of great value in the design and simulation process.

ACKNOWLEDGMENTS

The author extends her appreciation to those supervisors, coworkers, and associates who participated directly or indirectly in the work on which this report is based and/or in preparation of the report itself. More particularly, thanks to Mr. H. E. Crecraft, Dr. M. C. Carlson, and Mr. J. J. Koffley for their support and many helpful suggestions in reviewing the report draft, and to Mr. E. V. O. Drinkard for his editorial assistance.

LITERATURE OBTAINED

A complete file of vendor documentation used in technical analysis and in the preparation of this report is maintained at the NRL Ships Electronic Warfare Branch, Tactical Electronic Warfare Division. Requests to access this material should be made to Ms. Lynn Keuthan at AV 297-5937 (COM 202-767-5937).

ABBREVIATIONS AND ACRONYMS

ADT	Analog Design Tools
Apollo	Workstation platform (Hewlett-Packard)
ASCII	American Standard for Code Information Exchange
ASIC	Application Specific Integrated Circuit
C	High-level software language (developed by Kernighan and Ritchie)
CAD	Computer-aided design
CADAT	Simulator (HHB Systems)
CAE	Computer-aided engineering
CAM	Computer-aided manufacturing
CASE-VANGUARD	Schematic capture and PCB layout (Teradyne)
CMOS	Complimentary metal oxide semiconductor
DAS	Digital Analysis System (Tektronix)
DDSC	Database Designer's Schematic Capture (Tektronix)
DEC	Digital Equipment Corporation
EDIF	Electronic Design Interface Format
ERC	Electrical Rule Checker (Teradyne)
ESD	Engineering Services Division (NRL)
EW	Electronic Warfare
HI-CHIP	Hardware Modeler (GenRad)
HILO-III	Logic-simulation software package (GenRad)
IC	Integrated circuit
I/O	Input/output
LASAR	Logic Simulator (Teradyne)
LCC	Leadless chip carrier
LOGIX-SL	Logic-simulation software package (Silvar-Lisco)
Micro-CARDS	CAD/CAM software package (Scientific Calculations)
MIL SPEC	Military specification
MIT	Massachusetts Institute of Technology
MPC	Message Passing Coprocessor chip (Intel)
Multibus II	Standard bus backplane (Intel)
NFS	Network File System
MIP	Millions of instructions per second
NRL	Naval Research Laboratory
PADS PCB	CAD software package (CAD Software)
PAL	Programmable Array Logic
PALASM	Program to generate PAL fuse maps
PC	(1) Personal Computer, (2) Workstation platform
PCAD	PC computer software (Personal CAD Systems)
PCB	Printed-circuit board
PGA	Pin-grid array
PLD	Programmable logic device
PROM	Programmable read-only memory
PSPICE	Analog simulator software (Based on SPICE)
RAM	Random-access memory
RFI	Request for Information
RFP	Request for Proposal
ROM	Read-only memory
SCICARDS	CAD/CAM software package (Scientific Calculations)

SOP	Small outline package
SPICE	Simulator software (University of California at Berkeley)
SQL	Structured Query Language
SUN	Workstation platform (Sun Microsystems, Inc.)
Susie	Logic-Simulation package (ALDEC)
TEW	Tactical Electronic Warfare (NRL)
TSSI	Test Systems Strategies, Inc.
ULTRIX	Operating System (Digital Equipment Corporation version of UNIX)
UNIX	Operating system (AT&T Bell Labs)
VLSI	Very large scale integration
VMS	Operating system (Digital Equipment Corportion)
VUP	VAX Unit of Performance

Appendix A

DIRECTORY OF VENDORS

CAD/CAM Vendors

Academi Systems
2418 Armstrong Street
Livermore, CA 94550

Accel Technologies
7358 Trade Street
San Diego, CA 92121

Advanced Microcomputer Systems
2780 S.W. 14th Street
Pompano Beach, FL 33069

Aida
5155 Old Ironside Drive
Santa Clara, CA 95054

Analog Design Tools
(Valid Logic Systems, Inc.)
1080 East Arquez Avenue
P. O. Box 3422
Sunnyvale, CA 94088

Aptos Systems
10 Victor Square
Scotts Valley, CA 95066

Artecon, Inc.
2431 Impala Drive
Carlsbad, CA 92008

Augat Interconnection Systems
40 Perry Avenue
Attleboro, MA 02703

AUTODESK, Inc.
2320 Marinship Way
Sausalito, CA 94965

Automated Systems
1505 Commerce Avenue
Brookfield, WI 53005

Bishop Graphics, Inc.
5388 Sterling Center Drive
Westlake Village, CA 91359

CAD Software
19 Russell Street
P. O. Box 1142
Littleton, MA 01460

Cadam
1935 North Buena Vista Street
Burbank, CA 91504

CADdy
3401 Algonquin Road
Suite 340
Rolling Meadows,IL 60008

CADKEY
27 Hartford Turnpike
Vernon, CT 06066

Cadnetix
5757 Central Avenue
Boulder, CO 80301

CAECO
270 Caspian Drive
Sunnyvale, CA 94088

Calay Systems
2698 White Road
Irvine, CA 92714

Calos
3419 Edison Way
Freemont, CA 94538

Case Technology, Inc.
2141 Landings Drive
Mountain View, CA 94043

Computervision
100 Crosby Drive
Bedford, MA 01730

Daisy Systems
700 Middlefield Road
Mountain View, CA 94039

Dasoft Design Systems
1827B Fifth Street
Berkeley, CA 94706

Data Development Corporation
1717 South Orange Avenue
Suite 200
Orlando, FL 32806

Design Computation, Inc.
10 Frederick Avenue
Neptune, NJ 07753

Douglas Electronics
718 Marina Boulevard
San Leandro, CA 94577

Futurenet/Data I/O Corp.
9310 Topanga Canyon Boulevard
Catsworth, CA 91311

GenRad, Inc.
300 Baker Avenue
Concord, MA 01742

Great SoftWestern
270 West Hickory Street
Suite 202
Denton, TX 76201

Hewlett-Packard, Inc.
1507 Page Mill Road
Palo Alto, CA 94304

HHB Systems
1000 Wyckoff Avenue
Mahwah, NJ 07430

IBM Corporation
400 Columbus Avenue
Valhalla, NY 10595

Innovative Computer-Aided
Technology, Inc.
14979 Prairie Avenue
Lawndale, CA 90260

Intergraph, Inc.
One Madison Industrial Park
Huntsville, AL 35807

Lucasfilm Limited
P. O. Box 2009
San Rafael, CA 94912

Mentor Graphics, Inc.
8500 S.W. Creekside Drive
Building 1
Beaverton, OR 97005

Omation
1210 East Campbell Road
Suite 100
Richardson, TX 75081

Optima Technology
900 Middlesex Turnpike
Building 5
Billerica, MA 01821

OrCad Systems, Inc.
1094 S.W. Baseline Street
Suite 500
Hillsboro, OR 97123

PAFEC, Inc.
5550A Peachtree Parkway
Technology Park, Atlanta
Norcross, GA 30092

Personal CAD Systems
1290 Parkmoor Avenue
San Jose, CA 95126

Phase Three Logic
P. O. Box 985
Hillsboro, OR 97123

Phoenix Data Systems
2500 Grant Road
Mountain View, CA 94043

Quadtree Software Corporation
(Will be Silocon West Corp.)
5150 E. Pacific Coast Highway
Suite 320
Long Beach, CA 90804

Racal-Redac, Inc.
4 Liberty Way
Westford, MA 10886

Royal Digital Systems
3600 West Bayshore Road
Palo Alto, CA 94303

Scientific Calculations, Inc.
7635 Main Street
Fishers, NY 14453

Shared Resources
3047 Orchard Parkway
San José, CA 95134

Silvar-Lisco, Inc.
1080 March Road
Menlo Park, CA 94025

SoftCircuits
701 N.W. 13th Street
Suite C-4
Boca Raton, FL 33432

Spectrum Software
1021 South Wolfe Road
Sunnyvale, CA 94086

Tektronix, Inc.
CAE Systems Division
700 Professional Drive
Gaithersburg, MD 20877-6026

Teradyne
Design & Test Automation
321 Harrison Avenue
Boston, MA 02118

Valid Logic Systems, Inc.
2820 Orchard Parkway
San José, CA 95134

Versacad
7372 Prince Drive
Huntington Beach, CA 92647

Viewlogic Systems
275 Boston Post Road, West
Marlboro, MA 01752

Visionics
343 Gibraltar Drive
Sunnyvale, CA 94089

Wire Graphics
95 Sherwood Avenue
Farmingdale, NY 11735

Vendors Supplying CAD/CAM Products, Documentation and Platforms

Aldec
3525 Old Conejo Road, #111
Newbury Park, CA 91320D

Digital Equipment Corporation
Continental Blvd. MK01/W83
Merrimack, NH 03054-9987

Interleaf, Inc.
10 Canal Park
Cambridge, MA 02141

Logic Automation, Inc.
P. O. Box 310
Beaverton, OR 97075

Sun Microsystems, Inc.
2550 Garcia Avenue
Mountain View, CA 94043

Xerox Corporation
800 Long Ridge Road
Stamford, CT 06904

APPENDIX B

Request-for-Information (RFI) Letter

Letter sent to suppliers requesting information for the CAD/CAE project.

Dear Sirs:

I am engaged in a feasibility study on CAD/CAE systems for the Naval Research Laboratory. The intended purpose of this study is to recommend a system with capabilities which we have identified as being necessary for utilization in the area of electronic warfare.

The items in the enclosed list have been identified as desirable in any proposed solution. Prospective vendors meeting our re-quirements must be identified for this study no later than 26 February 1988. This is a solicitation for information only, not a request for proposal (RFP). Our procurement cycle dictates actual purchase will be in approximately one year.

I will appreciate all material, including price information, and recommendations you might offer in order to make an informed recommendation to my customer. The concluding section of my report is a recommendation to purchase a particular CAE system.

If you have any questions, I can be reached at the Naval Research Laboratory, (202)767-5941.

Very truly yours,

/s/ Lynn M. Keuthan
Lynn M. Keuthan
Electrical Engineer
EW Systems Division

Appendix C

CAD/CAM REQUIREMENTS

A. Schematics Capture

1. Database Management of Schematics
2. Error Checking
3. Incremental Compilation
4. Interpage Connections of Large Schematics
5. Windowing, Pan and Zoom
6. System Block Design
7. Parts List Generation, Connections List Generation
8. Custom User-Defined Components
9. Standardized Engineering Drawings
10. High Upper Limits on Number Components, Pages, etc.
11. Ability to Support Multi-Page Schematics

B. Logic Simulation

1. Timing Diagrams/Verification
2. Physical Modeling Ability (68000, Z80, 8085, 8086)
3. Simulation of RAM/ROM/PLDSs
4. Fault Simulation
5. Behavioral Modeling
6. High-Level Language Interface

C. Printed-Circuit-Board Work System

1. PCB Layout from Schematic
2. Automatic Pinouts
3. Connector Positions
4. Tooling Holes
5. Area Isolation
6. Manual Routing
7. Ability to Display a Minimum of 64 Simultaneous Colors
8. Minimum Resolution of 1024X1024
9. Parts List Generation
10. Generate Standardized Netlist

11. High Upper Limits on Number of Components, Traces, etc.
12. PCB Output in Standard Gerber Format

D. Component Libraries

1. TTL 7400
2. TTL 5400
3. CMOS
4. MIL SPEC Versions
5. Microprocessor Models

E. Documentation

1. Integration of Schematics, Timing Analysis, etc., and Text for Technical Publications

F. Plotters/Printers

1. Support HP Plotters and/or Houston Instruments
2. Support Presentation-Quality Documentation

G. Miscellaneous

1. Integrated System
2. Training
3. *Operator Friendliness*
4. Upward Compatibility
5. Open Architecture
6. Simulation/Memory Output in ASCII Files
7. Interface to Test Equipment
8. Ability to Produce Engineering Drawings, A - E Sizes
9. Versatility: Ability to Support Digital Systems, RF Systems, Microwave, Mechanical and Additional S/W and H/W Needed for Support
10. Flexible Configuration/Platform
11. Low-Resource Loading: How Much Does the S/W Tax the System (Worst Case)?
12. Maintainability/Vendor Support
13. Outright Purchase of Hardware and Software/Low Maintenance

Appendix D

INTERNAL NRL MEMORANDUM

Interoffice memorandum prepared at the Naval Research Laboratory on 2 February 1988. It announces the demonstration of the Tektronix CAD/CAM system that was arranged for 9 February 1988.

(From) Code 5740

SUBJECT: CAD/CAM DEMONSTRATION

TO: Distribution

1. The Ships EW Branch is sponsoring a demonstration of Tektronix's CAD/CAM system. This will be held on Tuesday, 9 February at the Tektronix facility in Gaithersburg, MD. Directions will be made available outside the Ships EW Branch Office, (Rm 1305), at 0800 hours on Tuesday.

2. Tektronix will present their PCB package (Merlin-P) with integration to HILO-3 (logic simulation) from 0930 to 1230 hours. They will demonstrate integration to testing equipment through TSSI and their front-end and back-end layout integration to RF/Microwave design (SuperCompact) from 1300 to 1600 hours. Attendance is open for morning or afternoon demonstrations or both.

/s/ H. E. Crecraft
H. E. Crecraft
Head, SEWS Branch, TEWD

Distribution
[Not included in this appendix]

Appendix E

COMPARISON CHARTS

The numbering (A1-G13) of requirements in Fig. E1 in this appendix corresponds to the numbers listed in Appendix C. The degree to which a specific requirement is met is rated from 0 to 5 where 5 corresponds to a full meeting of requirements.

NO.	COMPANY NAME	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	B1	B2	B3	B4	B5	B6	C1	C2	C3	C4	C5	C6	C7	C8
1.	Accelerated Technologies	4	5	0	5	5	0	5	5	5	3	5	0	0	0	0	0	0	5	5	5	5	1	5	3	3
2.	Advanced Micro Systems	3	5	0	0	5	4	5	5	5	3	0	0	0	1	0	0	0	5	5	5	5	5	5	3	3
3.	Analog Design Tools	ANALOG DESIGN AND ANALYSIS ONLY																								
4.	AUTODESK, INC.	MECHANICAL DRAFTING PACKAGE ONLY																								
5.	Bishop Graphics	4	0	0	5	5	0	5	3	4	5	5	0	0	0	0	0	0	5	3	3	0	0	5	2	3
6.	CADdy	4	4	0	5	2	4	5	5	3	3	5	0	0	0	0	0	0	4	5	5	4	5	5	3	3
7.	Cadnetix	4	5	5	5	5	4	4	4	5	4	5	4	3	3	2	0	0	4	3	3	4	4	5	3	4
8.	CAECO	4	0	3	2	2	4	4	0	0	1	2	2	0	0	0	0	0	0	0	0	0	0	0	0	0
9.	Case Technology	ACQUIRED BY TERADYNE																								
10.	Computer Vision	5	5	5	5	5	0	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	1	4
11.	Design Computation	4	5	3	5	5	0	5	0	5	2	5	0	0	0	0	0	0	5	5	5	5	5	5	3	2
12.	FutureNet/Data I/O	4	5	0	5	5	0	4	5	5	3	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13.	G. E. Calma	2	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	3	4
14.	Great SoftWestern	0	5	5	5	5	0	5	5	5	4	5	0	0	0	0	0	0	0	0	0	5	5	5	5	3
15.	Hewlett-Packard	5	5	0	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5

Fig E1 — Companies vs requirements

NO.	COMPANY NAME	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	B1	B2	B3	B4	B5	B6	C1	C2	C3	C4	C5	C6	C7	C8
16.	Mentor Graphics	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	0	5	5	5	5	5	5	5	4
17.	Omation	4	5	0	5	4	0	5	3	5	3	5	0	0	0	0	0	0	5	2	2	2	2	5	1	2
18.	OrCad Systems	4	5	2	5	5	5	5	5	5	3	5	5	0	4	0	0	3	3	5	5	5	5	5	1	3
19.	Personal CAD Systems	4	5	4	5	5	0	5	5	5	3	5	3	0	0	0	0	0	5	5	5	5	5	5	3	3
20.	Racal-Redac	5	5	5	5	5	5	5	5	5	4	5	5	5	4	5	5	5	5	5	5	5	5	5	4	4
21.	Scientific Cal.	5	5	5	5	5	0	5	5	5	5	5	5	5	5	5	5	0	5	5	5	5	5	5	3	4
22.	Silvar-Lisco	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	4
23.	Spectrum Software	4	0	0	0	5	0	3	0	0	1	0	5	0	0	0	0	0	0	0	0	0	0	0	1	3
24.	Tektronix CAE Systems Division	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	4
25.	Teradyne	4	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	4	5	5	5	5	5	5	5	4
26.	Versacad	MECHANICAL DRAFTING PACKAGE ONLY																								
27.	Viewlogic Systems	4	5	0	3	5	5	4	5	2	4	4	3	2	3	0	0	0	4	3	1	1	0	0	2	3
28.	Visionics	4	5	0	3	0	0	5	5	5	3	5	5	0	0	0	0	0	5	5	3	5	5	5	1	3

Fig. E1 (Continued) — Companies vs requirements

NO.	COMPANY NAME	C9	C10	C11	C12	D1	D2	D3	D4	D5	E1	F1	F2	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13
1.	Accelerated Technologies	5	5	3	5	3	3	0	0	0	0	5	0	3	2	4	3	5	0	0	2	5	5	0	4	3
2.	Advanced Micro Systems	5	3	3	3	3	3	3	0	2	2	5	4	2	0	3	2	4	0	0	2	4	5	0	4	3
3.	Analog Design Tools	STRICTLY LIMITED TO ANALOG DESIGN AND ANALYSIS																								
4.	AUTODESK, Inc.	MECHANICAL DRAFTING PACKAGE ONLY																								
5.	Bishop Graphics	2	0	5	5	0	0	0	0	0	0	3	0	2	0	2	0	3	0	0	0	5	4	3	4	3
6.	CADdy	5	3	3	5	0	0	0	0	0	4	5	3	3	3	3	3	4	0	0	4	5	0	5	4	3
7.	Cadnetix	5	5	5	5	4	4	4	4	2	2	5	4	4	4	3	3	3	0	0	4	3	5	2	2	4
8.	CAECO	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	2	0	0	3	2	0	3	4	3
9.	Case Technology	ACQUIRED BY TERADYNE																								
10.	Computer Vision	5	5	5	5	5	5	5	5	5	0	5	5	3	5	5	5	5	5	5	5	0	5	4	3	1
11.	Design Computation	5	5	3	6	2	2	0	0	0	0	5	1	2	0	5	3	5	0	0	2	5	5	0	4	3
12.	FutureNet/Data I/O	0	0	0	0	3	3	0	0	0	0	0	0	3	0	4	1	3	0	0	2	5	0	0	4	1
13.	G. E. Calma	5	5	5	5	5	5	5	4	2	3	5	3	3	3	3	0	1	5	3	2	2	5	0	3	4
14.	Great SoftWestern	5	3	3	5	3	1	3	0	0	0	5	5	1	4	4	3	4	0	0	3	5	5	0	4	2
15.	Hewlett-Packard	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	0	5	5	5	4	5	0	0	4

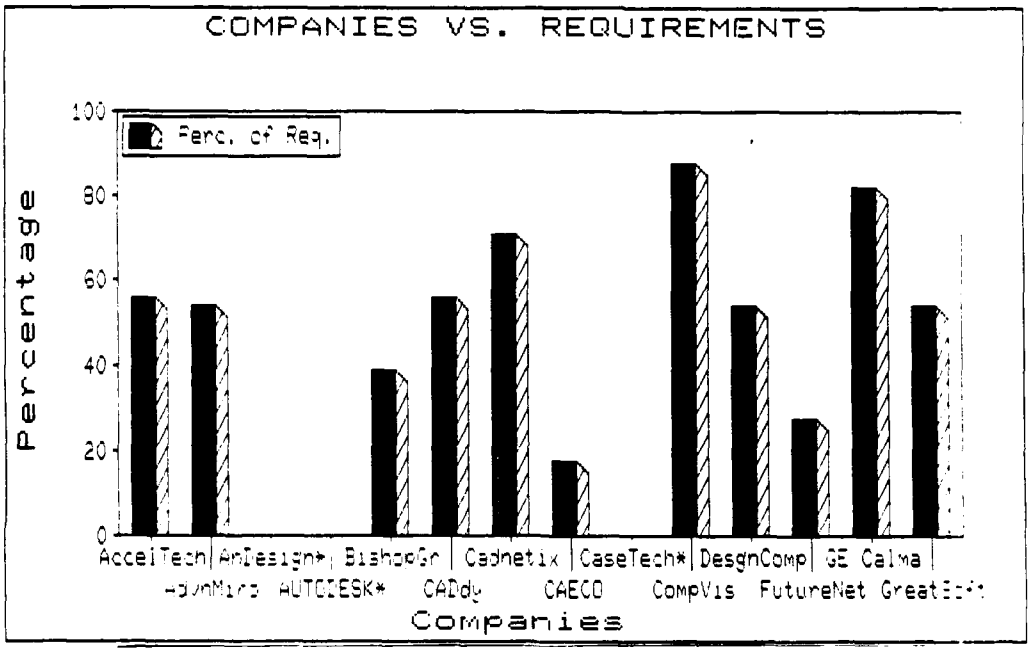
Fig. E1 (Continued) — Companies vs requirements

NO.	COMPANY NAME	C9	C10	C11	C12	D1	D2	D3	D4	D5	E1	F1	F2	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13
16.	Mentor Graphics	5	3	5	5	5	5	5	5	5	3	5	4	5	4	5	5	3	3	5	3	2	5	0	2	2
17.	Omation	5	3	3	5	4	3	3	0	3	0	5	0	2	0	4	4	4	0	0	3	5	5	3	4	1
18.	OrCad Systems	5	5	2	5	4	4	4	0	0	0	2	0	3	0	5	3	5	0	0	5	5	5	0	4	4
19.	Personal CAD Systems	5	5	3	5	4	4	3	0	2	0	4	0	3	5	3	3	4	0	0	4	3	5	0	4	3
20.	Recal-Redac	5	4	5	5	5	5	5	5	3	5	5	5	5	4	5	5	5	5	5	4	5	5	3	5	3
21.	Scientific Cal.	5	4	5	5	5	5	5	5	5	0	5	4	5	3	5	5	4	0	0	3	1	5	0	4	3
22.	Silvar-Lisco	5	5	5	5	5	5	5	5	5	0	5	3	5	5	4	5	5	3	3	4	4	5	3	4	4
23.	Spectrum Software	0	0	0	0	2	2	0	0	0	0	4	0	1	0	5	3	5	0	0	1	3	0	0	4	4
24.	Tektronix CAE Systems Division	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
25.	Teradyne	5	5	5	5	5	5	5	5	5	2	5	3	3	3	3	4	4	5	5	4	3	5	0	5	3
26.	Versacad	MECHANICAL DRAFTING PACKAGE ONLY																								
27.	Viewlogic Systems	5	5	4	0	3	3	0	0	0	2	2	0	1	0	3	3	4	0	0	3	0	2	0	4	0
28.	Visionics	5	5	3	5	3	2	3	0	0	0	5	0	1	0	4	3	4	0	0	2	4	5	3	4	0

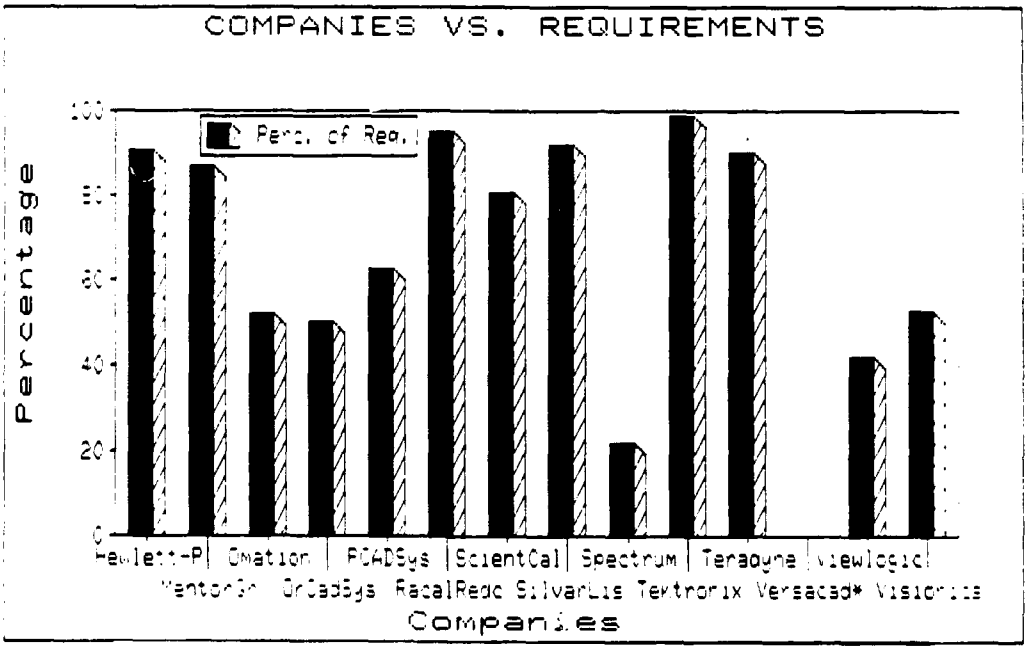
Fig. E1 (Continued) — Companies vs requirements

Appendix F

COMPARISON GRAPHS



Graph No. 1



Graph No. 2

Appendix G

RELATIVE PRICING

The following tabulation presents, in the order of fulfillment percentage of Naval Research Laboratory requirements, the estimated costs of the various CAD/CAE systems analyzed in the program covered by this report.

Company	Meets Reqts. (%)	Price (est.)	Maint. (if. appl.)
Tektronix	100	$56,000	$11,000
Racal-Redac	95	189,500	20,772
Silvar-Lisco	92	105,000	20,100
Hewlett-Packard	91	201,611	11,172
Teradyne	90	249,300	8,622
Computer Vision	88	253,859	28,602
Mentor Graphics	87	250,000	25,000
G. E. Calma	82	106,235	14,688
Scientific Calculations	81	100,000	17,000
Cadnetix	71	105,900	11,000
Personal CAD Systems	63	22,780	6,920
Accel Technologies	56	1,490	50
CADdy	56	2,370	350
Advanced Micro Systems	54	700	50
Design Computation	54	5,375	275
Great Softwestern	54	NO RESPONSE TO PRICING	
Visionics	53	5,730	250
Omation	52	2,794	N/A
OrCad Systems	50	495	N/A
Viewlogic Systems	42	9,500	950
Bishop Graphics	39	4,490	50
FutureNet/Data I/O	28	3,990	875
Spectrum Software	22	1,790	N/A
CAECO	18	97,000	10,000

Appendix H

APPLICATION NOTE

by William D. Billowitch, Executive Vice President, Quadtree

Successful Board-Level Simulation Depends on Accurate Models

If you have ever designed a logic board and had the experience of having to wait for device samples to arrive before you could debug the board or became frustrated when wire-wrap boards were assembled improperly (or when pins 1-8 and 9-16 of an IC socket were wired in reverse), or you had to fight to keep your favorite oscilloscope or logic analyzer from being "borrowed" by your friend in the other lab, you can appreciate the benefits of simulating your board design rather than developing the breadboard.

In fact, many design and analysis decisions can be more easily handled through the use of logic simulation rather than through more commonly used techniques. For example the problem of running the design over temperature or voltage to assure the design will work when stressed under actual operating conditions.

Steps in Logic Simulation

With low-cost schematic entry stations and powerful supermicro workstations or shareable supermini server processors, board-level logic simulation is in reach of every digital designer.

Performing board-level logic simulation on a workstation is not much different in principle than doing test bench debugging. The difference is that different tools are used to accomplish the task.

The first step is to describe the design to the logic simulator. Unless you enjoy writing lengthy "from-to" lists of each component's interconnectivity to other components, you begin by creating a schematic of the circuit on the workstation screen in an analogous manner to drawing it on paper. This involves using the CAE system's schematic capture software package. Once the circuit diagram is entered it is easily modified and you can generate draftsman-quality drawings from a plotter.

Most schematic capture packages perform an adequate job of allowing you to enter drawings. However, you may want to consider a few areas when making your selection:

- How much of a circuit can be viewed at once?
- How long does it take to pan or move a view of the drawing from one area to another?
- How easy is it to move components on the screen? Do the connections snap into the correct position when moved?
- Can components and connections be easily duplicated or copied?
- Can symbols be easily created and entered into the schedule?

As with a physical breadboard, a test fixture needs to be developed. On the laboratory bench, this may take the form of a test driver circuit as part of the test fixture and/or waveform generators connected to the circuit to represent actual input data.

Test patterns are developed by using a logic simulator in a similar fashion:

(a) By constructing a simulated driver circuit

(b) By specifying the applied test patterns using a test vector language, or on some systems,

(c) By actually drawing the applied waveform that the CAE system then applies to the specified input connection on the board.

Programmable devices such as PROMs or PALs need to be assigned their values. PROM and PAL programmers are used on the laboratory bench for this purpose. First, assembly language code is developed by the designer or software engineer. Once developed, it is assembled into executable machine code and then partitioned into separate PROM files as required. The PROMs are then burned from these files. PALs are designed by using PAL descriptive languages, CUPL, ABLE, or PALASM. These tools are used to minimize logic equations and in turn generate JEDEC files used to burn the PALs. As with any fuse programmable device, once it is programmed, generally it cannot be reprogrammed. EPROMs and UVPROMs of course, can be reprogrammed.

Simulation models of PROMs and PALs accept data in an identical way to that of their physical counterparts; however, instead of being "burned" with a fixed data set, they simply read their configuration from easily modifiable computer files. PAL and PROM models can be reprogrammed by changing the data on their associated files.

Now that the circuit has been entered, test vectors written, and programmable device files generated, the circuit is ready to simulate. The logic simulation will compile the circuit and link all of the models associated with the component symbols entered into the schematic. The result will be an executable simulator for the circuit. Running the simulator will force values on certain inputs as described by the test vectors. This in turn will cause the models to react to the stimulation and produce a response that is then propagated to other connected components to simulate the functionality and timing characteristics of the board.

The designer is able to probe the board to view waveforms and signal values in a manner similar to that used by a logic analyzer when probing a circuit to display its waveform. Unlike a logic analyzer, however, no glitches will go unnoticed since the simulated logic analyzers in most CAE tool sets have a bandwidth equal to the simulator's timing resolution that is generally less than 1 ns. Also, the trace depth of simulated logic analyzers is virtually unlimited. Triggering is automatic and allows every signal to be monitored.

Modeling Choices

A surprising 80% to 90% of those designing application-specific integrated circuits (ASIC) for the first time breadboard their designs by using off-the-shelf TTL or CMOS ICs and then map those devices to the equivalent macrocells of the ASIC foundry. Macrocell simulation of the ASIC is then performed to assure a functional chip upon fabrication. The high percentage of designers performing breadboards seems to indicate a lack of confidence in the tools provided, or initial trepidation with a new design methodology.

Successful logic simulation leads to repeated use of CAE logic simulation. However, a poor first experience could easily lead the designers back to the lab breadboards. Accurate models and easy-to-use tools are the key.

Model vendors can offer any of three types of models:

Structural models - developed by drawing a circuit diagram of the model according to other simpler models called primitives. Primitives are usually single "and""or""flip-flop" models that describe the fundamental functionality of those simple circuit elements. An R-S flip-flop can be structurally modeled, as shown in Fig. H1.

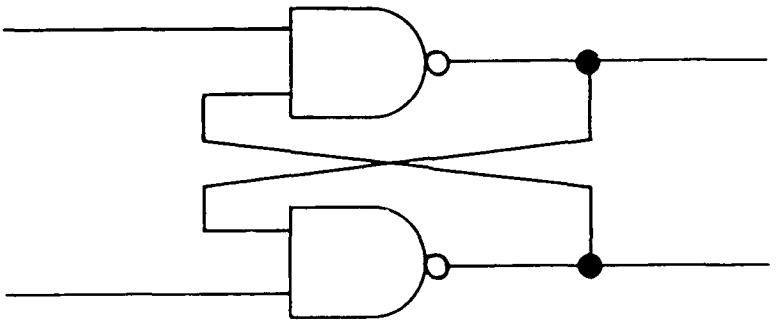


Fig. H1 — R-S Flip-flop structural model created from 2-input NAND grate primitives

Structural models are simple to build if the gate-level schematic of the device is available. However, the price to pay for this simplicity is their slower execution speed. And, microprocessor gate-level models are impractical and unavailable.

Behavioral models - overcome many of the size and speed disadvantages characteristic of structural models. Behavioral models require much more understanding of the functionality of the model by the model builder than would be required to build a structural model and provide an elegant solution to complex device modeling. Figure H2 shows a behavioral model of a 4-bit up/down counter. The internal variable "COUNT" holds the current count value until the next positive clock edge. Then, depending on the value of the up/down control time, the counter will increment or decrement its value or respond with an error message in the event the U/D line exhibits an unknown value.

```
Model 4-bit-counter,
PINS
   Q3,Q2,Q1,Q0   = OUTPUT;
   CLK,UD        = INPUT;
VAR
   COUNT = INTEGER;/*internal counter*/

When CLK   Then {
IF (UD = 1)  Then
   COUNT = (Count + 1) MOD 16;
   ELSE if (UD = 0)  Then
   COUNT = (Count - 1) MOD 16;
   ELSE X_ERROR ("U/D is UNKNOWN");
   Q3 = (COUNT/8) MOD 2;
   Q2 = (COUNT/4) MOD 2;
   Q1 = (COUNT/2) MOD 2;
   Q0 = COUNT MOD 2;

}
```

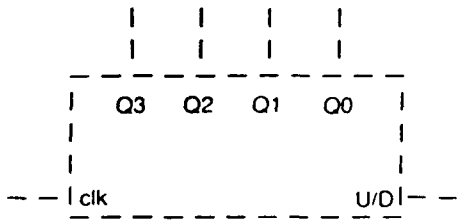


Fig. H2 — 4-Bit UP/DOWN counter

Had this model been developed structurally, it would have involved at least four flip-flops and quite a few gate-level models. The complexity of the model would have been greater and would consequently run slower.

Hardware models - use the actual device as the simulation model. Hardware models take the form of a plug-in printed-circuit card upon which sits the device being modeled and some additional control logic to interface to the device. This card is then installed in a computer peripheral called a hardware modeler that can contain a number of hardware models. Usually, the limit is 32 or so VLSI-class devices that can be accommodated in a hardware modeler.

The advantage of this type of model is that the actual device is used; therefore, it represents an accurate model of the device. Yet, the timing accuracy of hardware modelers is limited by economic factors and has been shown, in some cases, to have a negative influence on the device's accuracy as a model.

Nevertheless, hardware models are a good choice when a complex model is needed and an accurate software model is unavailable.

In terms of speed, hardware models run at close to or actual hardware speeds within the hardware modeler. But the hardware modeler is also busy scheduling all of the other hardware models for execution and needs to communicate with the simulator. All of this necessay protocol slows down the response time of the hardware modeler to the equivalent speed of software models. In fact, little observable execution speed difference exists between 10 Mhz or 1 Mhz hardware modelers or between these and a well written software behavioral model.

Most logic simulation users generally have a combination of the three modeling styles. Each type of model is satisfying a particular need.

Accuracy is the Key

Accurate models are essential for the success of board-level logic simulation. Without accurate models, designers will spend a great deal of their time debugging circuits only to find that the models were causing the problem. Then, unlike developing an IC where simulation is mandatory, the board-level designer is tempted to retreat to the laboratory where confidence has been established.

Designers need the confidence of knowing that the models are accurate. And, to obtain the highest level of accuracy available, the models must be certified by the integrated circuit manufacturer who developed the device.

Quadtree is the only model vendor to offer certified models. Certification means that the IC manufacturer and Quadtree have agreed to provide Quadtree with the confidential information necessary to assist in developing the model and then to perform the final model testing and thereby certifying its accuracy.

In many cases, Quadtree offers certified models even before the actual devices are available.

CERTIFIED

Certification reflects the highest standard of accuracy used by the industry to define the levels of confidence in model performance. Certification means that the device manufacturer of the corresponding model has agreed with the modeling company to fully test and certify that the models faithfully emulate

their actual devices. In many cases, certified models will be available even before the device samples are available from the IC manufacturer, thereby allowing the digital designer to design the latest devices into products sooner.

VERIFIED

Verification reflects the second highest standard of accuracy used by the industry to define levels of confidence in model performance. Verification means that the device manufacturer of the corresponding model has provided the modeling company with detailed proprietary information about the modeled device, including in many cases, test patterns but has not signed an agreement requiring they state the models have been certified.

VALIDATED

Validation reflects the third highest standard of accuracy used by the industry to define the levels of confidence in model performance. Test vectors are used that were developed with expert understanding of the functions and timing characteristics of each device. Validated models are sometimes subjected to tests that have been previously tested for accuracy. Validated models are directly compared to the actual device by using a hardware modeler and represent the state of the art in behavioral model testing when verification or certification is unobtainable.

Figure H3 shows the certified model development cycle.

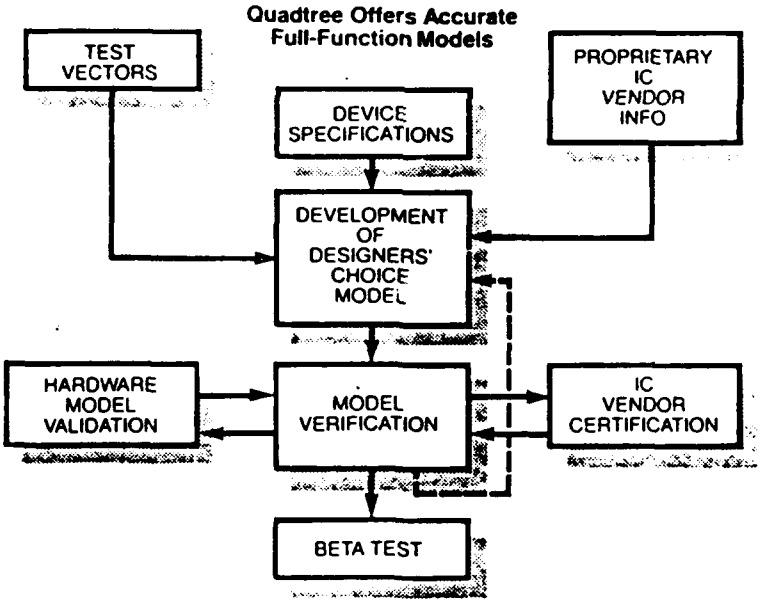


Fig. H3 — Certified quadtree model development cycle

Designers' Choice

Designers have many options in selecting appropriate systems for their needs. The choices will factor in cost, accuracy, and customer support. In an industry that changes so rapidly, it is best to evaluate carefully each vendor for its long-term commitment to the highest quality of products and for its support to customers throughout the design phase.

Appendix I

SYSTEM DESIGN AND DEVELOPMENT TOOLS, COMPUTER DESIGN

Worst-Case Timing Analysis Ensures Board Reliability*

By Lauro Rizzatti and Mary Wasilewski

By accounting for component performance variations, worst-case timing analysis uncovers errors that wouldn't be discovered during breadboarding.

As printed circuit board designers continue pushing the limits of circuit performance, they face the increasingly critical and demanding chore of verifying the timing of new designs. The potential for timing problems that can devastate product-development timetables multiplies when designing a complex VLSI board, where custom and semicustom ICs interact with standard off-the-shelf components in a dense, high-speed environment.

Subtle timing problems that produce marginal performance and intermittent failures are not apparent during the design and may not become evident until after volume production is in full swing and enough boards have gone through the test cycle to produce some meaningful statistics. Such marginality and intermittent failures can severely depress production yields, tie up expensive technicians in difficult and time-consuming board diagnosis, and saddle a vendor with a high rate of field failures. In a fast-moving and highly competitive market, such problems can turn a promising new product into a costly failure.

Timing errors must therefore be identified and corrected before a design is released to production. Manual timing analysis of board designs containing tens or hundreds of thousands of gates, however, is a time-consuming task. And a hardware prototype—since it is only one physical implementation of the design—does not tell the designer whether the design can tolerate all the timing interactions that can occur as components vary independently within their timing-specification range.

Some measure of a board's timing performance can be provided by software tools for timing verification, which analyze the topology of a design and calculate delays along the various paths in a circuit to predict likely timing problems. But these tools provide only a partial verification since they do not include any analysis of a circuit's logic states. A timing verifier may analyze the circuit as though all data paths were enabled all the time, for example. In actual board operations, though, some paths can not be enabled when other paths are active.

Because so many timing parameters are state-dependent, only a timing analysis that is performed as an integral part of logic simulation can ensure that board timing will be correct in actual operation. Although this combined logic simulation and timing analysis requires additional time and effort during design, it results in a faster move into volume production and, thus, a shortened time-to-market. This process also ensures higher levels of product quality and reliability.

The authors are applications engineers in the Design and Test Automation Group of Teradyne (Boston, MA).

Full worst-case timing analysis, a relatively compute-intensive process, does not have to be a part of early logic simulations, when a design is evolving rapidly. To get a rough measure of timing performance at some intermediate stage of design, an engineer might simulate the design by using only typical timing values. Once the design has been fine-tuned and is considered near its final form, however, a complete worst-case simulation using minimum and maximum timing values provides final design verification.

Structural and Functional Timing

The first requirement for combined logic simulation and worst-case timing analysis at the board level is a simulation model of the board. This includes models of each component on the board, and net-list information of how the components connect one to another.

Generally, designers use a mix of modeling levels. Although board parts may be modeled at the transistor level, they are more commonly modeled at higher levels (gate, functional or behavioral) to reduce simulation run time and memory requirements. When software models are not available, hardware modeling may also join the lineup with the electrical responses of a real device being incorporated into the simulation.

The modeling language's ability to represent timing parameters accurately at every modeling level depends on whether or not it can express timing parameters and values functionally as well as structurally. IC designers might model timing structurally, assigning independent delay values to each primitive within the device. But, board designers have no internal timing information on most of the components on a board; they have only the pin-level—or functional—timing data available from a vendor's spec sheet.

Functional timing parameters include input-to-output propagation delays, wire and loading delays, and input-to-input timing constraints such as setup and hold of data relative to the clock. Even when a device's structural timing is known, the functional timing information found on a spec sheet is valuable for true worst-case timing analysis because it reflects margining to account for lot variations and minor mask changes as well as for the range of operating specifications.

Modeling Functional Timing

The more device models a designer can pull from the simulator's library, the better, since these models typically include functional timing information. The designer will have to model devices not available in the model library. The vendor's spec book will likely include several pages of functional timing information, including pin-dependent and state-conditional delay values. A modeling language flexible enough to let the designer include all relevant information into the timing model helps ensure accurate timing analysis.

An essential aspect of modeling flexibility is the ability to model minimum, typical, and maximum delay values based on device technology and fan-out. CMOS devices, for example, are extremely load-sensitive, and the simulator should be able to automatically calculate the appropriate minimum, typical, and maximum delays individually for each device based on the load being driven.

To achieve greatest modeling efficiency, the designer must specify functional device timing, generically and specifically. Generic specifications quickly characterize timing behavior common to a particular device type, such as a 7474 flip-flop. But because a device's timing characteristics vary according to the technology used—Low-Power Schottky, Advanced Schottky or Fairchild Advanced Schottky technology, for instance—these generic timing specifications should be expressed by using

variables. Thus the designer can plug in the exact timing values, once the device technology has been decided.

By using variables to describe generic timing, a board designer can quickly tailor the timing model to account for components purchased to fit custom specifications. Should component availability dictate a parts-list change, this process can also make it easy to update the simulation model.

In addition to using variables, a designer may need to use algebraic expressions to create a flexible, yet precise, timing model. Using algebraic expressions and variables to describe load and wire delays, for example, lets a simulator's model compiler keep track of distributed loads along all the circuit's interconnections and factor them automatically into the simulation.

Algebraic expressions and variables also accommodate back-annotation of the simulation model after board layout. As VLSI boards become denser, the importance of modeling exact wire delays based on actual physical layout is becoming as important at the board level as it is for large ICs. If a simulator can replace estimated values with actual delays from a board-layout CAD system, the analysis is made more accurate because the error-prone process of reprogramming these values manually has been eliminated.

Two other valuable tools for modeling functional timing are pin-dependent and state-conditional statements. These let the timing model reflect that multiple propagation paths often exist through a device. If restricted to the use of a single value for the delay through the device, the designer is forced to average all the path delays into a nominal minimum/maximum value. As a result, the accuracy of the timing model is degraded. Pin- and state-conditional expressions, on the other hand, let the simulator calculate the exact delay range that is possible depending on the path along which the device propagates a signal.

Along with load, wire, and I/O propagation delays, the designer must model input-to-input timing constraints such as data setup and hold relative to the clock, or minimum pulse widths allowable on clock, clear and preset pins. Pin- and state-dependent modeling statements make this process more precise and let the designer check device input-pin timing relative to activity on other inputs.

A final, critical element of the timing model is a timing description of the backplane or system in which a board or module eventually will operate. Because of unforeseen timing interactions with the off-board circuitry, even an apparently perfect board design can fail. Thus the simulation model should reflect the backplane's contribution to the timing uncertainty (skew) that accompanies every signal it receives back from the board. This process ensures that the final product will work as intended in the system environment.

Worst-Case Timing Analysis

Accurate simulation and timing analysis of the completed board model imposes other concerns on the designer. Obviously, the goal is an analysis rigorous enough to identify any and all the timing hazards such as races, spikes, and setup-and-hold violations. At the same time, the analysis should not report hazards that do not exist. If the designer can not trust the analysis and must double check each timing-hazard report to determine whether it is real, the value of the timing analysis is greatly diminished—or is eliminated altogether—since designers will not use an unreliable tool.

True worst-case timing analysis—one neither too optimistic nor too pessimistic—requires simulation not only of all component and interconnect delays on the board at their minimum values but again at their maximum values. The real worst-case scenario for a board will almost certainly be one

in which some components are operating at the minimum end of their specification ranges while others are running at the maximum end. Thus, every possible minimum/maximum combination on the board must be simulated and analyzed.

Prior to simulation, the designer develops a set of stimuli that the simulator applies to the inputs of the circuit model. These stimuli will test the logical and timing functions of the board. The simulator analyzes timing by tracking the progress of every signal through the circuit and by meticulously calculating the minimum and maximum amounts of delay that accumulate along the way. The simulator uses this information to compute the earliest and latest arrival times possible for each signal at each node in the circuit. At device inputs for which timing constraints are specified, the simulator checks for illegal conditions and for timing hazards such as setup-and-hold violations.

The simple process of adding up delays, however, ignores several factors that limit the amount of delay that can accumulate in a physical board. Worst-case timing analysis, therefore, must include a consideration for these factors. Otherwise the simulator will output a barrage of false timing-hazard reports that may take days or even weeks to track down and dismiss.

Three simulation techniques keep timing analysis from becoming overly pessimistic: common-ambiguity removal, correlation and glitch analysis. Of these, common-ambiguity removal screens out the largest category of apparent (but unreal) timing hazards.

Phantom hazards appear when the timing uncertainty produced by minimum/maximum delay values along signal paths becomes so large that events appear to overlap. The only way the simulator can determine whether the hazard is real is by evaluating the relative timing of the events and discounting the common ambiguity arising from shared delays in reconverging signal paths. A typical example of common ambiguity occurs when two signals propagate through the same component. The simulator duly adds this component's minimum-to-maximum timing uncertainty to the accumulating skew of each signal. When the signals reconverge further along in the circuit, that common ambiguity may give the appearance of overlapping events.

At this point, the simulator must be able to trace back along all circuit paths to identify the common component and subtract its contribution to each signal's skew. Theoretically, this process is possible because the simulator has been storing every logic-state transition throughout the simulation. But tracking back through many levels of logic in a complex VLSI board design is a considerable analytic chore. To be efficient, the simulator should launch a common-ambiguity search only when it encounters an apparent hazard. This search should be automatic, and a hazard report should be withheld until the simulator has judged whether the hazard is real or not.

Correlation techniques applied to board-level timing analysis take into account the fact that some minimum/maximum combinations simply don't occur in the real world. Gates fabricated on common silicon—as in a gate array—track one another to some extent; one won't operate with maximum delay while its neighbor operates at minimum. Nor will one path through a device propagate signals at the high end of its minimum/maximum delay spec while another path propagates signals at the low end of its range.

To avoid an overly pessimistic analysis, therefore, a designer needs to specify a percentage of correlation between signals propagating through the same device package. This correlation specification reflects the fact that any one device will operate within some smaller-than-worst-case range across several signals.

Dealing With Glitches

Because glitches will inevitably occur, the designer must simulate these random events realistically during board design. If it automatically propagates every glitch no matter how narrow, the simulator can easily slip into an overly pessimistic analysis, which may result in false timing-hazard reports.

Although many glitches produce no effect, simply instructing the simulator to ignore any glitch with a pulse width narrower than some specified value leaves the designer blind to glitches that could affect board performance. The best solution is a compromise. The simulator should respond to each glitch by reporting an unknown state (x), and by propagating the x state through the circuit. Because only the designer can ultimately decide whether the glitch will really cause a problem, the simulator should also issue a hazard report.

When the simulator must report a timing hazard, designers will save a considerable amount of time if they can have a detailed description of the hazard. This description should use the same symbolic node and signal names included in the circuit model and tell the designer where the hazard has occurred. It should also describe the type of hazard, when it occurred, the margin of error, and the fan-in/fan-outs for the inputs and outputs involved.

Graphic representation on a terminal display screen of hazard input signals, such as waveforms, helps the designer visualize circuit activity. This representation also greatly simplifies the understanding and tracing of a hazard to its source.

Weighing Costs and Benefits

Traditionally, designers have been evaluated based on how quickly their designs get into production, so anything that adds time and effort to the design cycle needs very solid justification. Certainly, simulation with full worst-case timing analysis requires more of the designer's time than does hardware prototyping. Even though it extends one phase of design, however, simulation with worst-case timing verification pays for itself in several important ways. By catching timing problems early, this process minimizes the time and cost of the multiple hardware prototypes typically required to debug complex board designs.

Finally, simulation data generated during timing verification can be used in functional board-test programs and diagnostics. The stimulus and response patterns output by the simulator serve as a convenient means of communicating the designer's performance specifications to the test department, giving test engineers a head start on generating high-quality test programs.

Simulation and timing analysis are impossible without models for every device on a board. Although a simulator's model library contains many device models, models for complex VLSI parts typically are not available. Yet creating structural level models from scratch for such components may literally take several engineer-years.

Behavioral models that describe only the functionality of a device or a logic block, provide a way out. They can be easily written by using a manufacturer's published specs. Also, behavioral models simulate far faster than strucural models.

Benchmark results indicate that substituting a behavioral model for a structural model of a VLSI microprocessor or support chip, for example, can cut overall board-simulation time in half. And using a hardware model instead of a structural model can make the simulation run 10 to 20 times faster.

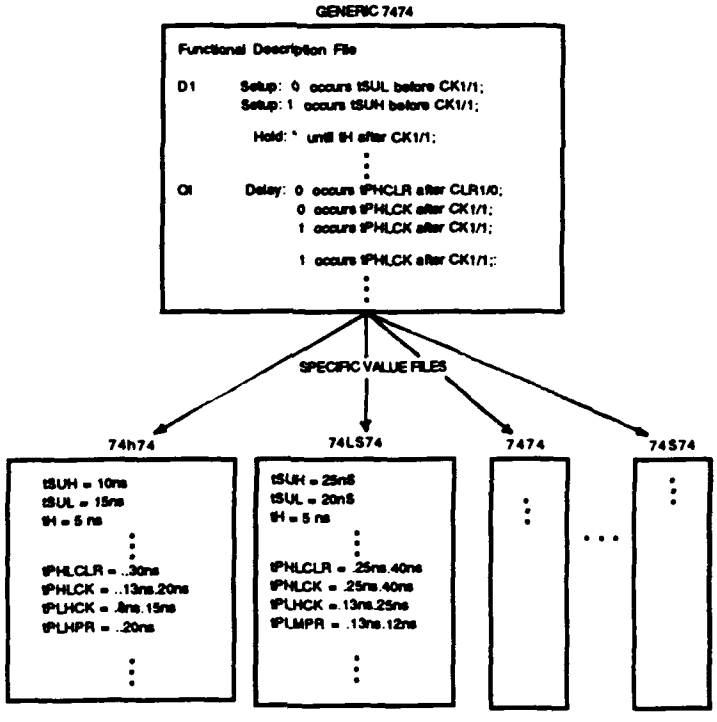


Fig. I1 — Access to both generic and technology specific expressions of functional timing charactiristics and values lets designers tailor a timing model based on the device technology used or on components purchased against custom specifications. The designer simply replaces generic values as needed with values from a manufacturer's spec sheet.

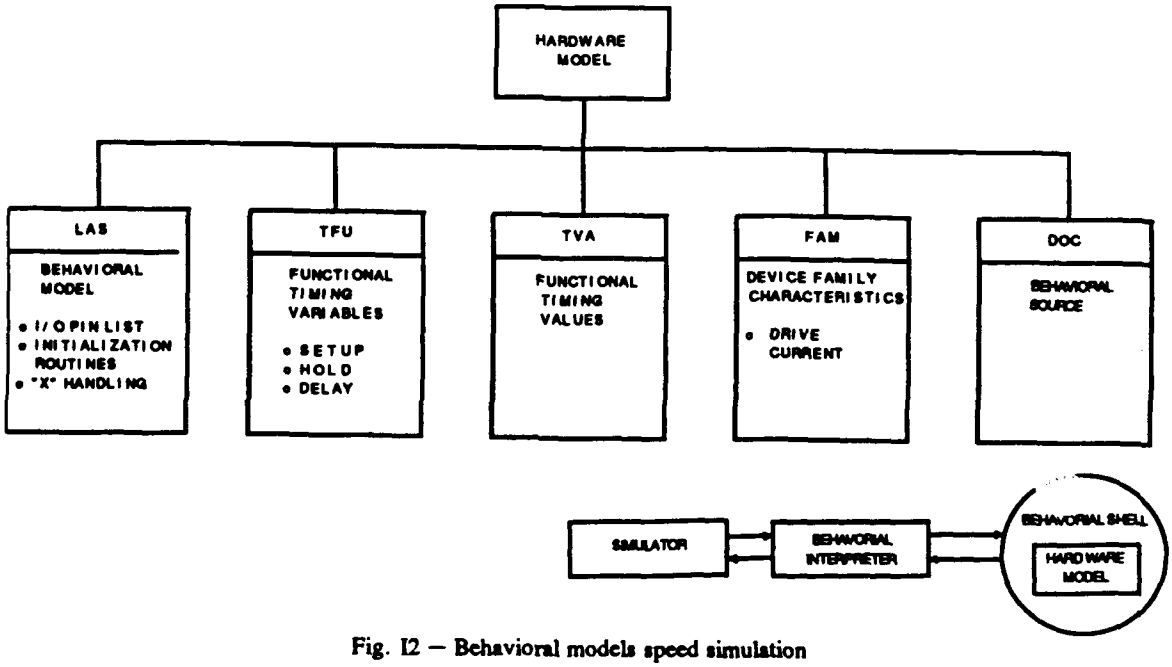


Fig. I2 — Behavioral models speed simulation

Two prerequisites exist for accurate worst-case timing analysis during simulations in which behavioral models are used. The simulator must be able to model and simulate functional timing descriptions, and the behavioral modeling language must support propagation of x (unknown) logic states as well as the standard 0, 1, and z (tristate) logic values through the behavioral model. Since timing hazards such as races or setup-and-hold violations will cause a device's output to become unknown, the simulator's ability to propagate x states to the appropriate output pins of a behavioral model alerts a designer to the problem.

Hardware models by themselves do not support true worst-case timing analysis because a single physical copy of a device cannot express the part's full range of minimum/maximum timing. Moreover, a simulator flags timing hazards by propagating x's when component outputs become unknown, but a physical device cannot produce x's--only 1s and 0s.

Designers can solve the first problem by creating a software description of functional timing parameters and minimum/maximum values based on the vendor's spec sheet for the device. The simulator can then use this description for all timing evauations, referencing the hardware model itself only for logical responses.

Thus, the simulator can perform minimum/maximum and full worst-case timing analysis. It can also simulate full-board performance over a wide range of input timing parameters without requiring elaborate hardware to supply these various inputs physically to the hardware model.

To compensate for the hardware model's inability to propagate x states, the designer uses a behavioral language to write a behavioral shell. Residing in the simulator's model library along with the functional timing files on the device, this behavioral shell contains I/O pin list information, device initialization requirements and rules for propagation of x states through the device when unknown or illegal inputs are received.

By letting the simulator propagate x states correctly and use device responses only when the hardware model is properly initialized and synchronized, the behavioral shell ensures accurate, repeatable timing analyses based on simulations using a hardware model.

When board designers at Teradyne's Manufacturing Systems Division began simulating their boards by using the Lasar Version 6 simulation system, they unanimously reported that flagging timing errors was Lasar's most valuable contribution. While timing flaws occurred less frequently than logic errors, their tendency to make the design fail intermittently--or fail in worst-case situations--made them far more difficult and tedious to diagnose. As a result, the engineers welcomed a tool that could automate that chore.

A typical example of marginal performance involved a board on which pulses were created by using the propagation delay of several components. Lasar's worst-case timing analysis revealed to two designers something that they had failed to consider: the pulse could be too narrow if all the components were operating at the fast end of their specifications.

Another designer discovered that what he had assumed to be a sound design (based on simulation using typical timing values) proved to be marginal when subjected to a true worst-case analysis. The designer found that the register's setup requirements were violated if data arrived at a register slower than the typical time but still well within the allowable minimum/maximum range. The design also could not tolerate a faster-than-typical arrival of a latch-enable at the register.

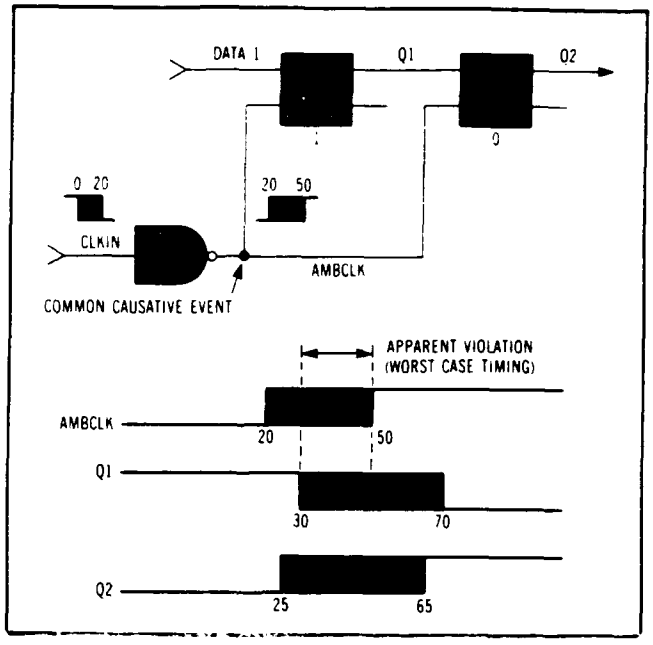


Fig I3 — Shared delays in reconverging signals cause a condition called "common ambiguity" during worst-case timing analysis. In this example, it is not clear from the AMBCLK and Q1 waveforms whether a 0 or 1 will be locked at flip-flop 0. But a look at the circuit's topology reveals that 30 ns of ambiguity stems from a common source. By removing this ambiguity, Teradyne's Lasar simulator finds that stable data is being clocked into the flip-flop, yielding the waveform shown for Q2.

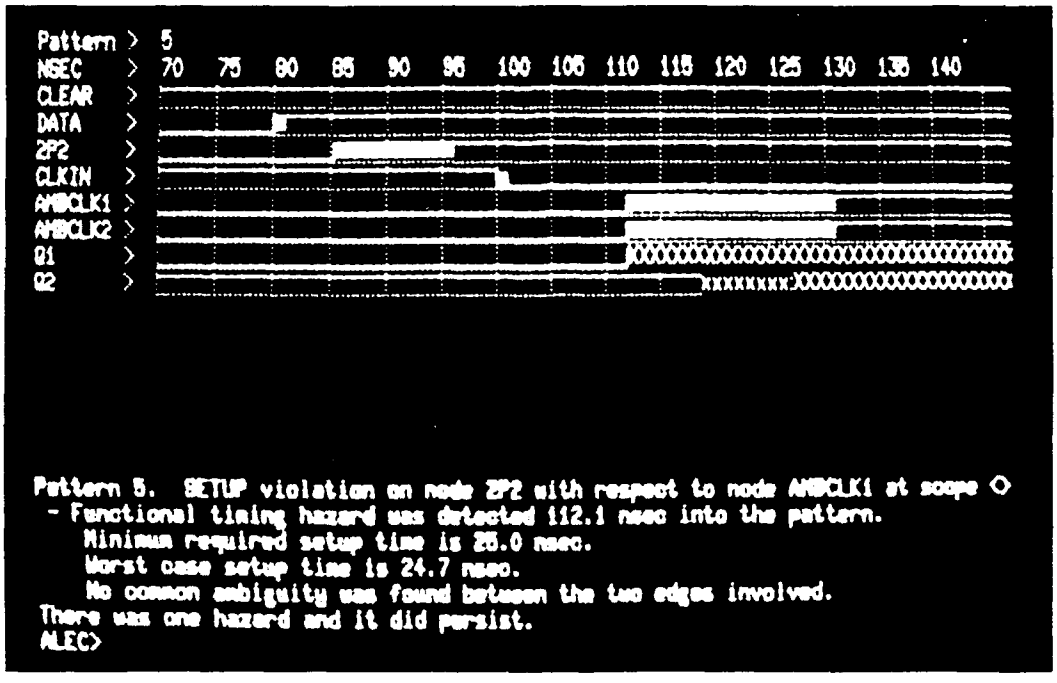


Fig. I4 - Designers find value in worst-case timing analysis

In another case, the output of a multiplexer was to provide data to a flip-flop. But, in certain circumstances, this multiplexer produced a glitch. Worst-case timing analysis determined that this glitch could occur too close to the clock signal, thus violating the flip-flop's setup time requirement.

For each timing hazard, Lasar issued a hazard report that included both a detailed description and a graphic representation of the hazard. With these reports, the designers could understand and quickly correct the timing problems.